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学　位　論　文　題　目	Bit Error Rate Simulation Models for Large-Scale Cross-Point Memories （和訳：大規模クロスポイントメモリーにおけるビット誤り率のシミュレーションモデル）
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【論文審査】Review of the thesis

This thesis aims to propose bit error rate (BER) simulation models for large-scale cross-point memories and to verify their validity for practical purposes. The thesis focuses on BER, which has not been predicted for cross-point memories, though BER is one of the most important parameters to design the error correcting code (ECC) for realizing high-density products, and the Resistive random access memory (ReRAM) is one of the most promising candidates for the replacement of NAND Flash memory, which is widely used for data storage in information products. When ReRAM is composed of cross-point arrays, it offers the potential for large-scale data storage with a smaller cell size than that of NAND Flash memory. In a cross-point array, memory elements are sandwiched between orthogonally patterned word-lines (WLs) and bit-lines (BLs). Thus, cell sizes of $4F^2$ are possible, where F is the feature size of a technology node, making cross-point arrays suitable for high-density ReRAM. The proposed models are applicable to any type of cross-point memory, including ReRAM and magnetic random access memory (MRAM),

because the cross-point array is composed of memory elements in which the resistivity can be changed by applying an electric current. Both ReRAM and MRAM suffer disturbances at the non-selected address while data are being written to the selected address. The BER caused by these disturbances can be calculated by the proposed models. As these two memories have different device parameters that affect the disturbance, this thesis investigates the effect of the device parameters on the BER for ReRAM and MRAM.

The thesis consists of 11 chapters. i.e., “Chapter 1:Introduction”, “Chapter 2: Issues to realize large-scale cross-point memory”, “Chapter 3: Estimation of bit error rate”, “Chapter 4: Fast computation of cell current using advanced simplified circuits”, “Chapter 5: Verification of the proposed simplified circuits”, “Chapter 6: Calculation sequence”, “Chapter 7: Reduction in the BER using error correcting code ”, “Chapter 8: Reduction in the BER using error correcting code”, “Chapter 9: Device design of MRAM”, “Chapter 10: Conclusions”, “Chapter 11: List of research achievements”.

In Chapter 2, two major issues preventing the realization of large-scale cross-point memories are discussed . The first is the trade-off relationship between the disturbance and the write error, and the second is the long calculation time of the cell current. Thus, a fast computation technique for the cell current in the cross-point array is required to enable the design of the large-scale cross-point memories.

In Chapter 3, a numerical solution for the BER in cross-point memories is introduced. The BER caused by the disturbance and the write error can be calculated using a two-dimensional probability density function. The algorithm is based on a comparison of the switching threshold current and the cell current. The distributions of the switching threshold current and the cell current are a result of process deviations and the selected address. The solution takes the deviation current into account and thus represents a comprehensive tool for optimizing the BER.

In Chapter 4, new simplified circuits are proposed. These provide a fast computation technique for the cell current in the cross-point array. The conventional simplified circuit has been widely used for calculating the worst-case cell current, with the calculated address assumed to be located at the array corner, where the metal wire length is greatest. Thus, the calculated cell current is reduced by the wire resistance, giving the

worst case for the write operation. However, read disturbances can occur when the read current is greater than the switching threshold current. The conventional simplified circuit cannot estimate this large read current, which may flow across any address in the cross-point array. Moreover, write disturbances can occur at the non-selected and half-selected addresses when a datum is written to the selected address. Again, the conventional simplified circuit cannot estimate this disturbance current, which may also flow across any address in the cross-point array. Therefore, simplified circuits for estimating the read disturbance current and the write disturbance current are proposed for fast computation with cross-point arrays.

In Chapter 5, the proposed simplified circuits are successfully verified by comparing the calculated cell currents with those in the original circuits. The results indicate that the simplified circuits give an accurate representation of the cell currents.

In Chapter 6, calculation sequences are described in detail. The calculation sequence for estimating the BERs induced by disturbances and write errors has been described. The sequence is composed of six steps. Consequently, the BERs caused by disturbances and write errors are obtained. The calculation time for 1000 loops of Steps 1–5 was 6.46 s. In addition, it took 1.11 s for Step 6 to obtain each BER. The proposed sequence is sufficiently fast that it represents a comprehensive tool for the design of large-scale memory.

In Chapter 7, Calculation results, the simulation results reveal that the trade-off relationship between the disturbance and write error limits the BER. There are two bias schemes in the write cycle, namely the $V_{DD}/2$ scheme and the $V_{DD}/3$ scheme. The $V_{DD}/3$ scheme leads to larger operating margins than the $V_{DD}/2$ scheme. This is because the applied voltage in the non-selected cell in the $V_{DD}/3$ scheme is less than that in the $V_{DD}/2$ scheme. However, as both cases produce large BERs, the current production line cannot provide any commercial products.

In Chapter 8, a Bose–Chaudhuri–Hocquenghem (BCH) code, (a highly efficient ECC), is applied to a 1Gb ReRAM to rescue the failing bits. It is found that the 1 Gb ReRAM has a sufficient operating margin under the $V_{DD}/3$ scheme with a BCH code of length $n = 64$ with $t = 4$, where t is the number of correcting bits in the code. The proposed simplified

circuits constitute a comprehensive tool for developing low-cost memory chips matching current production lines.

In Chapter 9, the design of MRAM devices is discussed in the same manner as for ReRAM. MRAM is also composed of cross-point arrays, and the trade-off relationship between disturbance and write error must be considered. By using the BCH code of length $n = 64$ with $t = 4$, the respective operation windows of the 1 Gb MRAM are calculated as a function of α, which is defined by the shape of the asteroid curve. To obtain the operation window with $\sigma = 10\%$, α should be less than 0.3. This is the target for low-cost memory chips with current production lines. Two different MRAM cells are proposed for decreasing α. The target α can be realized by these two proposed cells.

The significance of this thesis is that the proposed models are able to estimate the precise BER and design cross-point memories by applying the ECC to secure the desired BER. The conventional method has a limitation: it cannot calculate the BER. The proposed BER models reveal that the trade-off relationship between disturbance and write error is one of the most critical issues affecting cross-point memories. The originality of this thesis lies in the proposal of new simplified circuits to approximate the current flowing through the non-selected cells and the establishment of BER simulation models using statistical methods. The conventional simplified circuits cannot calculate the non-selected cell current. The proposed models are comprehensive tools for designing large-scale cross-point memories.

To calculate the BER in cross-point memories, it is necessary to estimate the cell current flowing through the memory array using Kirchhoff's laws. However, it takes a long time to calculate the current when the array size is large. For instance, it takes 33 days to calculate the current in an array with 4096 WLs and 4096 BLs, and then, a simplified circuit has been widely used to speed up the calculation. However, the conventional simplified circuit cannot determine the current at all addresses of the array because it is designed to predict the minimum current due to the wire resistance *IR*-drop. To overcome this limitation, new simplified circuits are proposed that obtain the current at all addresses of the array. The proposed simplified circuits can calculate the current at the half-selected and non-selected addresses in addition to the selected address. Therefore, the BER due to disturbances can be estimated. These disturbances occur at

the half-selected or non-selected addresses while data is being written to the selected address.

The BER models proposed in this thesis use a two-dimensional distribution of two variables: the cell current and the switching threshold current. The probability of the write error is numerically calculated by integrating over the region in which the write current is smaller than the switching threshold current at the selected address. In the same manner, the probability of the disturbance can be obtained by integrating over the region in which the half-selected or the non-selected cell current is larger than the switching threshold current. The proposed simplified circuits constitute effective BER models because they give the current distribution. By using the proposed BER models, appropriate ECCs were designed for the realization of large-scale cross-point memories.

The originality of this thesis lies in the proposal of new simplified circuits to approximate the current flowing through the non-selected cells. Based on these circuits and statistical methods, BER simulation models were established. The proposed models are comprehensive tools for the design of large-scale cross-point memories.

This thesis covers a narrow range of applicable criteria, and there is a need for further study in this area. This thesis assumes linear characteristics, steady states, and two-dimensional memories. In the future the proposed models in this thesis will be expanded to non-linear characteristics,, transition state, and three-dimensional memories. In an actual device, the non-linear characteristics, and the transition phenomenon are often seen. The non-linear characteristics can be applied to Kirchhoff's laws using iterative methods. It is possible to analyze the transition state using capacitance simulation. The three-dimensional memories have already been commercialized in NAND flash memory and PCM, and are becoming the de facto standard. In the three-dimensional memories, the sneak current increases according to the hierarchy, so it is important to predict the BER caused by disturbance.

The BER simulation models proposed in this thesis provides the guide to produce the large-scale cross-point memories. This thesis leads to the conclusion that the efficient ECCs are required for the cross-point memories because the trade-off relationship between disturbance and write error is one of the most critical issues to realize the large-

scale memories.

【審査結果】Summary and decision

The thesis entitled *"Bit Error Rate Simulation Models for Large-Scale Cross-Point Memories"* focuses on production of low-cost and high-density resistive random access memory (ReRAM) by preparing a statistical model to estimate the bit error rate (BER).

The thesis proposes a statistical model to estimate the BER in ReRAM composed of cross-point arrays that are suitable for large-scale data storage. The proposed statistical model deals with the unique failure modes in the cross-point array and is intended to enable the development of low-cost, large-scale data storage products. As a result, the BER produced by the trade-off between the read disturbances and write errors is precisely predicted for unipolar writing memory. Furthermore, the model is successfully expanded to bipolar writing memory, which suffers from write disturbances in the half-selected and non-selected cells. This is the first attempt to estimate the BER caused by the trade-off between disturbances and write errors in bipolar writing memory as well as in unipolar writing memory.

Two first-authoring papers have been published by international journals : 1) IEICE Transactions on Electronics,vol. E99-C, no.1, pp.119 ～ 128,2016 and 2) IEICE Transactions on Electronics, vol.E100-C, no.3, pp.329-339,2017, and one co-authoring paper has been published by an international journal: IEICE Transactions on Electronics,vol.E100-C,no.3 pp.2757-2759, 2006.

Judging by the results shown in the thesis and the number of international papers published so far, the level of the present research results is definitely high by international standards and the present results may well make a great contribution to the development of cross-point memories for realizing low-cost non-volatile memory. In conclusion, the thesis is considered as a high quality, high standard one by international standards. Therefore, all the members of the review committee judge that this dissertation is worthy of a doctoral degree of Graduate School of Interdisciplinary New Science, Toyo University.