Toyo University Doctoral Thesis

Bit Error Rate Simulation Models for Large-Scale Cross-Point Memories

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Abstract

This thesis focuses on the bit error rate (BER), which has not been predicted for cross-point memories, though it is one of the most important parameters to design the error correcting code (ECC) for realizing high-density products, and the thesis aims to propose bit error rate (BER) simulation models for large-scale cross-point memories and to verify their validity for practical purposes.

Resistive random access memory (ReRAM) is one of the most promising candidates for the replacement of NAND Flash memory, which is widely used for data storage in information products as mentioned in Chapter 1. When ReRAM is composed of cross-point arrays, it offers the potential for large-scale data storage with a smaller cell size than that of NAND Flash memory. In a cross-point array, memory elements are sandwiched between orthogonally patterned word-lines (WLs) and bit-lines (BLs). Thus, cell sizes of $4F^2$ are possible, where F is the feature size of a technology node, making cross-point arrays suitable for high-density ReRAM.

The proposed models are applicable to any type of cross-point memory, including ReRAM and magnetic random access memory (MRAM), because the cross-point array is composed of memory elements in which the resistivity can be changed by applying an electric current. Both ReRAM and MRAM suffer disturbances at the non-selected address while data are being written to the selected address. The BER caused by these disturbances can be calculated by the proposed models. As these two memories have different device parameters that affect the disturbance, this thesis investigates the effect of the device parameters on the BER for ReRAM and MRAM.

As described in Chapter 2, there are two major issues preventing the realization of large-scale cross-point memories. The first is the trade-off relationship between the disturbance and

the write error, and the second is the long calculation time of the cell current. Thus, a fast computation technique for the cell current in the cross-point array is required to enable the design of the large-scale cross-point memories.

In Chapter 3, a numerical solution for the BER in cross-point memories is introduced. The BER caused by the disturbance and the write error can be calculated using a two-dimensional probability density function. The algorithm is based on a comparison of the switching threshold current and the cell current. The distributions of the switching threshold current and the cell current are a result of process deviations and the selected address. The solution takes the deviation current into account and thus represents a comprehensive tool for optimizing the BER.

In Chapter 4, new simplified circuits are proposed. These provide a fast computation technique for the cell current in the cross-point array. The conventional simplified circuit has been widely used for calculating the worst-case cell current, with the calculated address assumed to be located at the array corner, where the metal wire length is greatest. Thus, the calculated cell current is reduced by the wire resistance, giving the worst case for the write operation. However, read disturbances can occur when the read current is greater than the switching threshold current. The conventional simplified circuit cannot estimate this large read current, which may flow across any address in the cross-point array. Moreover, write disturbances can occur at the non-selected and half-selected addresses when a datum is written to the selected address. Again, the conventional simplified circuit cannot estimate this disturbance current, which may also flow across any address in the cross-point array. Therefore, simplified circuits for estimating the read disturbance current and the write disturbance current are proposed for fast computation with cross-point arrays.

In Chapter 5, the proposed simplified circuits are successfully verified by comparing

the calculated cell currents with those in the original circuits. The results indicate that the simplified circuits give an accurate representation of the cell currents.

Using the calculation sequence described in Chapter 6, the simulation results in Chapter 7 reveal that the trade-off relationship between the disturbance and write error limits the BER. There are two bias schemes in the write cycle, namely the $V_{DD}/2$ scheme and the $V_{DD}/3$ scheme. The $V_{DD}/3$ scheme leads to larger operating margins than the $V_{DD}/2$ scheme. This is because the applied voltage in the non-selected cell in the $V_{DD}/3$ scheme is less than that in the $V_{DD}/2$ scheme. However, as both cases produce large BERs, the current production line cannot provide any commercial products.

In Chapter 8, a Bose–Chaudhuri–Hocquenghem (BCH) code, (a highly efficient ECC), is applied to a 1Gb ReRAM to rescue the failing bits. It is found that the 1 Gb ReRAM has a sufficient operating margin under the $V_{DD}/3$ scheme with a BCH code of length $n = 64$ with $t = 4$, where t is the number of correcting bits in the code. The proposed simplified circuits constitute a comprehensive tool for developing low-cost memory chips matching current production lines.

In Chapter 9, the design of MRAM devices is discussed in the same manner as for ReRAM. MRAM is also composed of cross-point arrays, and the trade-off relationship between disturbance and write error must be considered. By using the BCH code of length $n = 64$ with $t = 4$, the respective operation windows of the 1 Gb MRAM are calculated as a function of α, which is defined by the shape of the asteroid curve. To obtain the operation window with $\sigma = 10\%$, α should be less than 0.3. This is the target for low-cost memory chips with current production lines. Two different MRAM cells are proposed for decreasing α. The target α can be realized by these two proposed cells.

The significance of this thesis is that the proposed models are able to estimate the

precise BER and design cross-point memories by applying the ECC to secure the desired BER. The conventional method has a limitation: it cannot calculate the BER. The proposed BER models reveal that the trade-off relationship between disturbance and write error is one of the most critical issues affecting cross-point memories. The originality of this thesis lies in the proposal of new simplified circuits to approximate the current flowing through the non-selected cells and the establishment of BER simulation models using statistical methods. The conventional simplified circuits cannot calculate the non-selected cell current. The proposed models are comprehensive tools for designing large-scale cross-point memories.

Contents

Chapter 1 Introduction

1.1 Background

1.1.1 Significance of large-scale memory in the electronics industry

Semiconductor memories[1] implemented by integrated circuits (ICs)[2] are one of the most important products in the electronics industry, and are widely used for digital information products such as computers. The worldwide market for semiconductor memories was worth US$77,205 million in 2015 [1], corresponding to 23.0% of the total semiconductor product market, as shown in Fig. 1.1. Thus, semiconductor memories have obviously played an important role in the electronics industry.

There are two major semiconductor memories in computers, namely dynamic random access memory (DRAM)[3] and NAND Flash memory[4]. DRAM works as a main memory that stores data and programs sent from a central processing unit (CPU)[5]. In contrast to this, NAND Flash memory works as a storage medium accessing DRAM. Note that hard disc drives (HDDs)[6] are also used for storage in computers. Both DRAM and NAND Flash are important devices in computers.

To realize fast computer operations, the CPU and memories should operate very quickly. However, as for memories, it would be expensive to use only a single high-speed, large-scale memory would be expensive. That is why the cost and performance of computers are optimized by combining some high-speed, small-scale memory modules with other low-speed, large-scale memories. The former include static random access memory (SRAM)[7] and DRAM. Whereas DRAM operates as the main memory, SRAM works as a cache memory[8] to decrease the difference in performance between CPU and main memory. The latter is NAND Flash memory working as storage. That is, in practice, the cost and performance of computers are optimized using the cache memories, main memories, and storage.

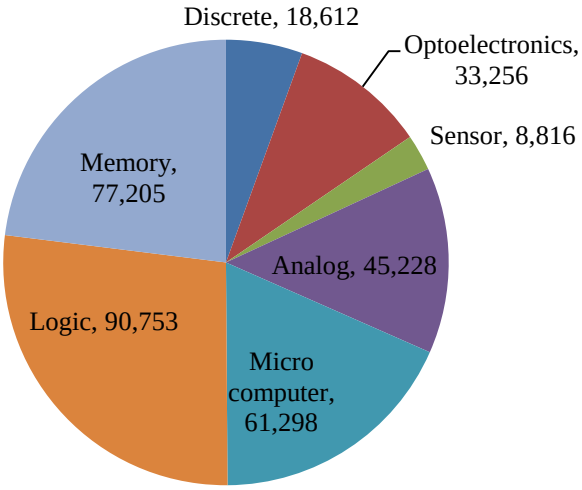


Fig. 1.1 Worldwide semiconductor market in 2015 [1]. Units are millions of US$. The portion corresponding to memory makes up 23.0% of the total.

1.1.2 Reason for high integration of memory

As the CPU speed rises with the development of high-performance transistors by CPU manufactures, large-scale memories are required to meet the requirements of CPU performance. To obtain large-scale memories, the memory modules themselves should be scaled down to smaller size. As the process feature size decreases, the number of memory chips that can be inserted onto each silicon wafer[9] increases. This can reduce the overall cost of the memory chip. For this reason, memory manufacturers have been developing process technology for reducing the physical size. The half-pitch trends of DRAM and NAND Flash memory are shown in Fig. 1.2 [2]. The half-pitch is defined as half of the most critical pattern pitch: the memory capacitor and word-line are the most critical patterns in DRAM and NAND Flash memory, respectively.

NAND Flash memory can be either two-dimensional (2D) or three-dimensional (3D)

[3]. As 2D NAND Flash memory faces scalability limitations, the 3D version has come to replace it. The half-pitches of DRAM and 3D NAND Flash memory have been decreasing in recent years to satisfy the demands of CPU performance.

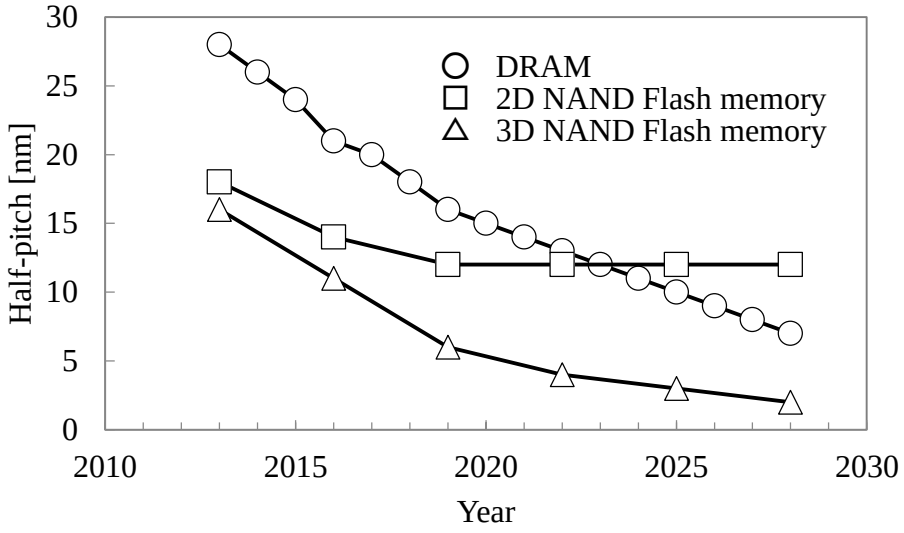


Fig. 1.2 Half-pitch trends of DRAM and NAND Flash memories [2]. The half-pitch of the 3D NAND Flash memory is equivalent to the square root of the cell footprint divided by two and then divided by the number of 3D layers.

1.1.3 Taxonomy of semiconductor memories

Memories used for electronics devices are generally categorized into two groups. The first group requires mechanical parts for reading and writing data, such as HDDs, compact discs (CDs)[10], digital versatile discs (DVDs)[11], and Blu-ray discs (BDs)[12]. The second group consists of semiconductor memories that are implemented by IC. Because they have no mechanical parts, semiconductor memories are low-power, high-density, high-speed, high-endurance, and vibration-resistant devices.

In terms of writing data, there are two types of semiconductor memories: random access memory (RAM) and read-only memory (ROM). These two types are explained below.

RAM is a memory device that allows data to be read or written at almost the same time at any addresses. DRAM and SRAM are examples of RAM devices. DRAM stores data in an array of capacitors. As the stored charge leaks to some degree, DRAM periodically requires a refresh cycle to recharge the capacitors. DRAM is a volatile memory[13] device because the stored data in the capacitors disappear after the supply power is switched off. In contrast, SRAM stores data in an array of flip-flops and requires no refresh cycle. SRAM is also a volatile memory device because the stored data in the flip-flops disappear once the power supply is switched off.

ROM is a type of non-volatile memory[14] that allows data to be read but not written during normal operation. For instance, in Mask ROM, data are programed in fabrication and cannot be programed by any users. Programmable ROM (PROM) is another type of ROM in which data are programed by a certain procedure. PROM is further categorized into four memories, such as one-time PROM (OTPROM), erasable PROM (EPROM), electrically erasable PROM (EEPROM), and Flash memory.

OTPROM allows data to be programed one time and does not allow data to be erased. Data programing is carried out using specific equipment. EPROM allows data to be programed and erased. There are two methods of erasing data in EPROM. Ultraviolet erasable PROM (UV-EPROM) erases data by irradiating ultraviolet rays, whereas EEPROM erases data using a tunneling phenomenon. The erase circuit is implemented on the chip.

Flash memory is a non-volatile memory device that allows data to be read, written, or erased. The erased data consist of a block[15]. Flash memory stores data in an array of floating-gate transistors, where the threshold voltage is raised by injecting hot electrons. Data cannot

be overwritten, because this would raise the threshold voltage incorrectly. To write data into an address that is already storing written data, the written data should be erased by pulling electrons from the floating gate to reduce the threshold voltage. NAND Flash memory [4][5] and NOR Flash memory[16] are different types of Flash memory. NOR Flash memory allows random access read, whereas NAND Flash memory allows only sequential access read inside one block. However, NAND Flash memory can achieve faster write speeds and has a larger capacity than NOR Flash memory. NAND Flash Memory is one of the most popular non-volatile memories because of its low cost, high density, and low power requirements. It is widely used for storage products such as smartphones, tablet PCs, solid state drives (SSDs)[17], and digital cameras. The various types of semiconductor memory are summarized in Fig. 1.3.

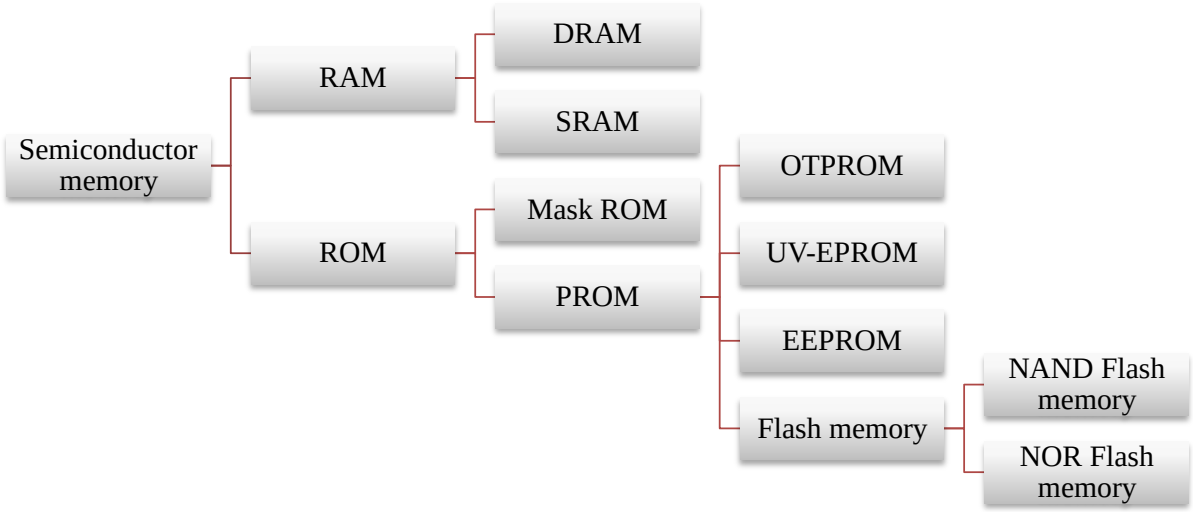


Fig. 1.3 Taxonomy of semiconductor memories.

1.1.4 Volatile and non-volatile memories

In subsection 1.1.3, one of the classifications between memory types was made from the viewpoint of writing data. There is a different classification method for semiconductor memory according to data retention, namely volatile memory and non-volatile memory. Volatile memory cannot retain data after the power has been switched off. Volatile and non-volatile memories correspond to RAM and ROM in Fig. 1.3, respectively.

DRAM and NAND Flash memory are the major types of volatile and non-volatile memories in the electronics industry, respectively.

1.1.5 Process integration issues of large-scale memory

DRAM has recently faced scalability limitations [6] because fine-size lithography processes require significant plant and equipment investment and it is increasingly difficult to retain enough capacitance to store data. The footprint of the capacitor decreases as the bit scale increases. Thus, the thickness of the capacitor insulator film must also shrink to ensure the same capacitance as in the previous generation. DRAM manufacturers are therefore developing thin and high-permittivity materials.

NAND Flash memory has also faced scalability limitations regarding fine-size lithography processes and operation margins [6][7]. The former is the same issue as faced by DRAM, whereas the latter is a result of capacitance coupling with adjacent cells. To overcome this limitation, 3D NAND Flash memory was proposed [3]. 3D NAND Flash memory offers an increase in bit capacity without fine lithography processing and without any degradation in reliability. NAND Flash memory manufacturers are now beginning to supply 3D NAND Flash memory products [8][9][10].

1.1.6 Emerging memories

Several emerging memory types have been studied for future non-volatile memories, such as phase-change memory (PCM)[18] [11][12][13], resistive random access memory (ReRAM)[19] [14][15][16], and magnetic random access memory (MRAM)[20] [17][18]. These all share the same read mechanism, although they have different write mechanisms. The memory elements consist of resistive material sandwiched between two metallic terminals, and the material resistance can be changed by applying a voltage. At least two resistance states exist. Data can be read and written by sensing the change of resistance and applying a voltage, respectively.

Of the emerging memories, PCM and ReRAM can be composed of cross-point arrays and are intended to replace NAND Flash memory. They offer a small cell size of $4F^2$, where F is the feature size. MRAM has a different memory cell structure, consisting of one transistor and one magnetic tunnel junction. MRAM is suitable for fast memory applications, such as DRAM.

The memory elements of PCM are usually made of $Ge_2Sb_2Te_5$. This can be transformed between crystal and amorphous phases by applying a voltage to the memory element. The crystal and amorphous phases exhibit low and high resistance values, respectively. The read current can be sensed at lower voltages than the phase transforming voltage so as not to destroy the stored data.

Several types of ReRAM have been reported. According to ITRS 2013 [19], these include electrochemical metallization bridge (EMB) ReRAM, metal oxide-bipolar filamentary (MO-BF) ReRAM, metal oxide-unipolar filamentary (MO-UF) ReRAM, and metal oxide-bipolar non-filamentary (MO-BN) ReRAM. These are categorized according to their switching mechanism and electrical characteristics.

EMB ReRAM is also called conductive bridge RAM (CBRAM) [20]. In the memory element, an ion conductor is sandwiched between two metals. One is an electrochemically active material, such as Ag or Cu, whereas the other is electrochemically inactive, such as W, Ta, or Pt. The resistance of the memory element is changed by the creation and de-creation of a conductive filament in the ion conductor [21]. When a positive voltage is applied to the electrochemically active metal, metal ions are formed by oxidation at the electrochemically inactive metal. These ions drift through the ion conductor to the electrochemically active metal, creating the filament. The filament is de-created by applying a negative voltage to the electrochemically active metal.

MO-BF ReRAM has a memory element in which a metal oxide is sandwiched by two metals. The resistance of the memory element is changed by the creation and de-creation of a conductive filament in the metal oxide, such as TaO_x or HfO_x. (Note that tantalum oxide and hafnium oxide are written as Ta_2O_3 and HfO_2, respectively, if their stoichiometry is known. However, the ratios are not specified here, and so they are written as TaO_x and HfO_x.) Some MO-BF ReRAMs have been released as commercial products [15][16].

MO-UF ReRAM, also called thermochemical memory (TCM), has the feature that SET[21] and RESET[22] operations can be performed by applying a voltage in the same direction. The memory element is composed of a metal, an insulator, and another metal, with NiO_x or HfO_x used as the insulator. The resistance of the memory element is changed by the creation and de-creation of a conductive filament in the insulator.

Unlike the other three ReRAMs, MO-BN ReRAM does not use a filament in the switching mechanism. The memory element is composed of perovskite, such as $PrCaMnO_3$ [22], and the switching current is proportional to the area of the memory element.

The emerging memories are summarized in Fig. 1.4 [19]. PCM, ReRAM, and MRAM

have been studied as candidates for the next non-volatile memory. This thesis examines the device design of ReRAM necessary to realize commercial products.

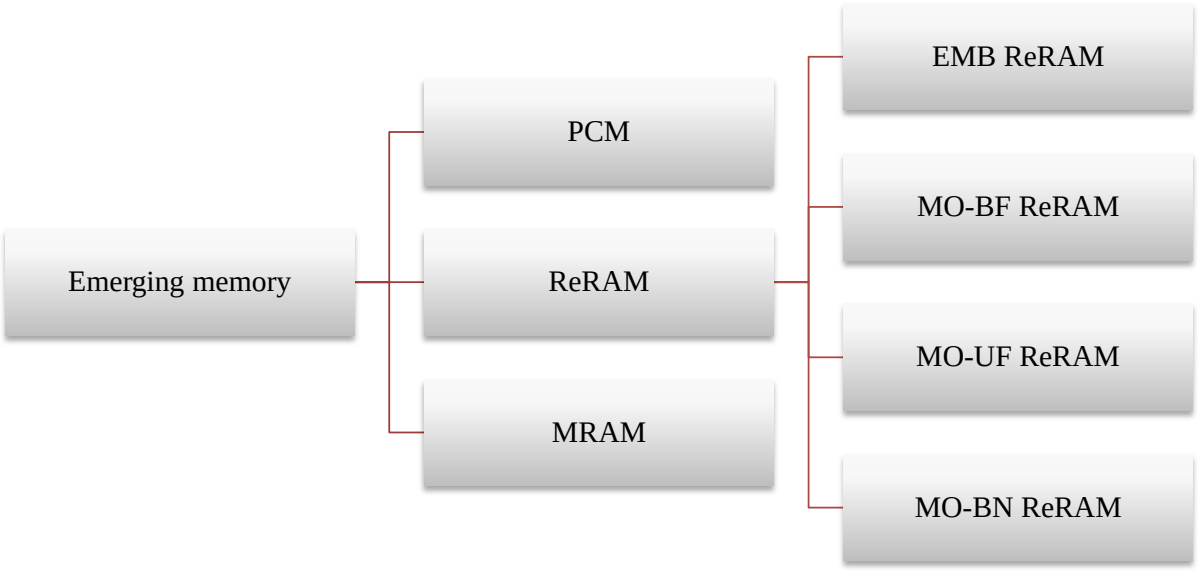


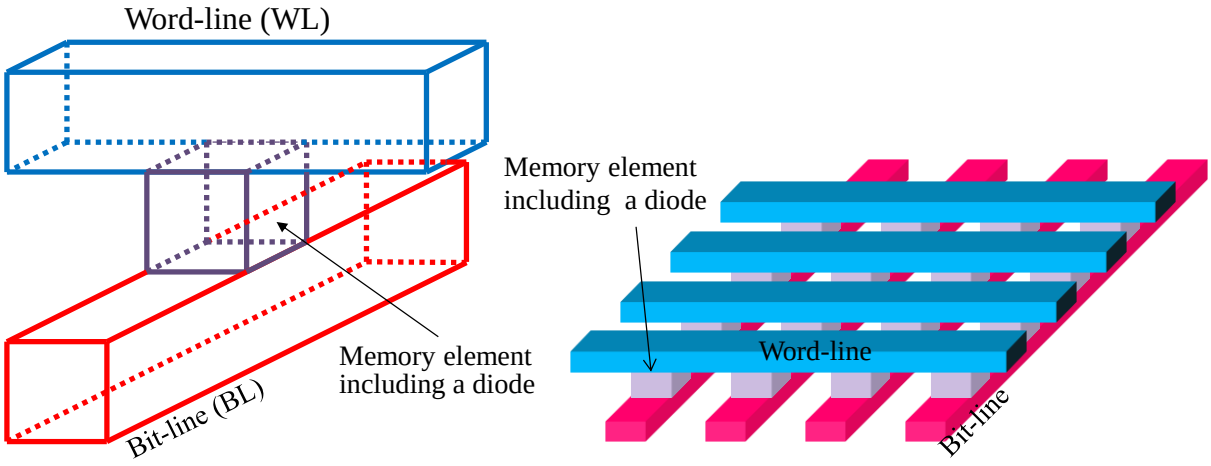
Fig. 1.4 Taxonomy of emerging memories.

1.2 Significance of cross-point memories

The emerging memories described in Subsection 1.1.6 have the potential for large-scale data storage with a smaller cell size than that of NAND Flash memories. This is because they are applicable to cross-point arrays. In cross-point arrays, memory elements are sandwiched between orthogonally patterned word-lines (WLs) and bit-lines (BLs), as shown in Fig. 1.5. Thus, cell sizes of $4F^2$ are feasible, where F is the feature size of a technology node. In addition, 3D memories are also feasible by using cross-point arrays. The emerging memories are intended for the design of large-scale memories using cross-point arrays.

Therefore, the cross-point arrays used for these emerging memories are studied in this

thesis with the aim of realizing large-scale data storage. Many studies have been reported on the cross-point array. However, there is currently no technique for estimating the bit error rate (BER)[23]. In this thesis, new failure rate simulation models are proposed for the realization of large-scale cross-point memories. This is because the BER is one of the most important parameters in the design of an error correcting code (ECC)[24]. The development of BER simulation models is a significant step in the design of an appropriate ECC for large-scale cross-point memories.



(a) Unit cell of cross-point memory. (b) Cross-point array.

Fig. 1.5 Cross-point memory.

1.3 Study objectives

This thesis proposes BER simulation models for large-scale cross-point memories and verifies their validity for practical purposes. By using the calculated BER, an appropriate ECC is designed for the realization of high-density products.

To calculate the BER, it is necessary to estimate a cell current flowing through the memory array using Kirchhoff's laws. However, it takes a long time to calculate the current

when the array size is large. Thus, optimized simplified circuits are proposed so as to obtain the current through a fast calculation. The proposed simplified circuits enable the current to be calculated at the half-selected and non-selected addresses in addition to the selected address. As a consequence, the BER due to disturbance can be estimated.

The proposed models are applicable to any cross-point memories including ReRAM and MRAM which are composed of memory elements in which the resistivity can be changed by applying an electric current. Accordingly using the proposed models, the operation window of ReRAM and MRAM is analyzed in terms of realizing large-scale memories. By using the calculated BER, an appropriate ECC is designed for ReRAM and MRAM.

To address these motivations, this study has the following contents:

1) Proposal of simplified circuits for fast computation of cell currents.

2) Proposal of a statistical method for estimating the BER of disturbances and write errors.

3) Introduction of the trade-off relationship between disturbances and write errors, which is one of the most critical issues in realizing cross-point memory.

4) Discussion of the calculation results for the trade-off relationship between disturbances and write errors.

5) Introduction of ECC into cross-point memory composed of cross-point arrays.

6) Presentation of design guidelines for optimizing the trade-off relationship using ECC in order to provide low-cost non-volatile memory products.

1.4 Chapter organization

To achieve the objectives described in the previous section, this study is organized as shown in Fig. 1.6. In Chapter 2, the main issue associated with realizing large-scale cross-point memory is reviewed, namely the trade-off relationship between disturbance and write error that

limits the BER. In Chapter 3, the statistical method of calculating the BER of disturbance and write error in the cross-point array is developed. Chapter 4 describes the new simplified circuits for the fast calculation of cell currents. This simplification is necessary because it takes a long time to calculate the cell current in cross-point arrays using the full circuit representation. In Chapter 5, these simplified circuits are verified against the original circuit. Chapter 6 discusses the calculation sequence for the BER. In Chapter 7, the BER of disturbance and write error are calculated as parameters of the resistance and threshold variations. Chapter 8 introduces an ECC for the cross-point memory with the aim of improving the BER. Design guidelines for the optimization of the trade-off relationship using the ECC are derived for low-cost non-volatile memory products. In Chapter 9, the device design of MRAM is discussed by estimating the BER, which is analogous with the cross-point array. There is a trade-off relationship between the half-selected disturbance and the write error in MRAM. It is demonstrated that the BER due to the trade-off relationship decreases when the BCH code is applied to MRAM. Finally, in Chapter 10, this study concludes by noting that the appropriate ECC would optimize the operation window of the cross-point memory.

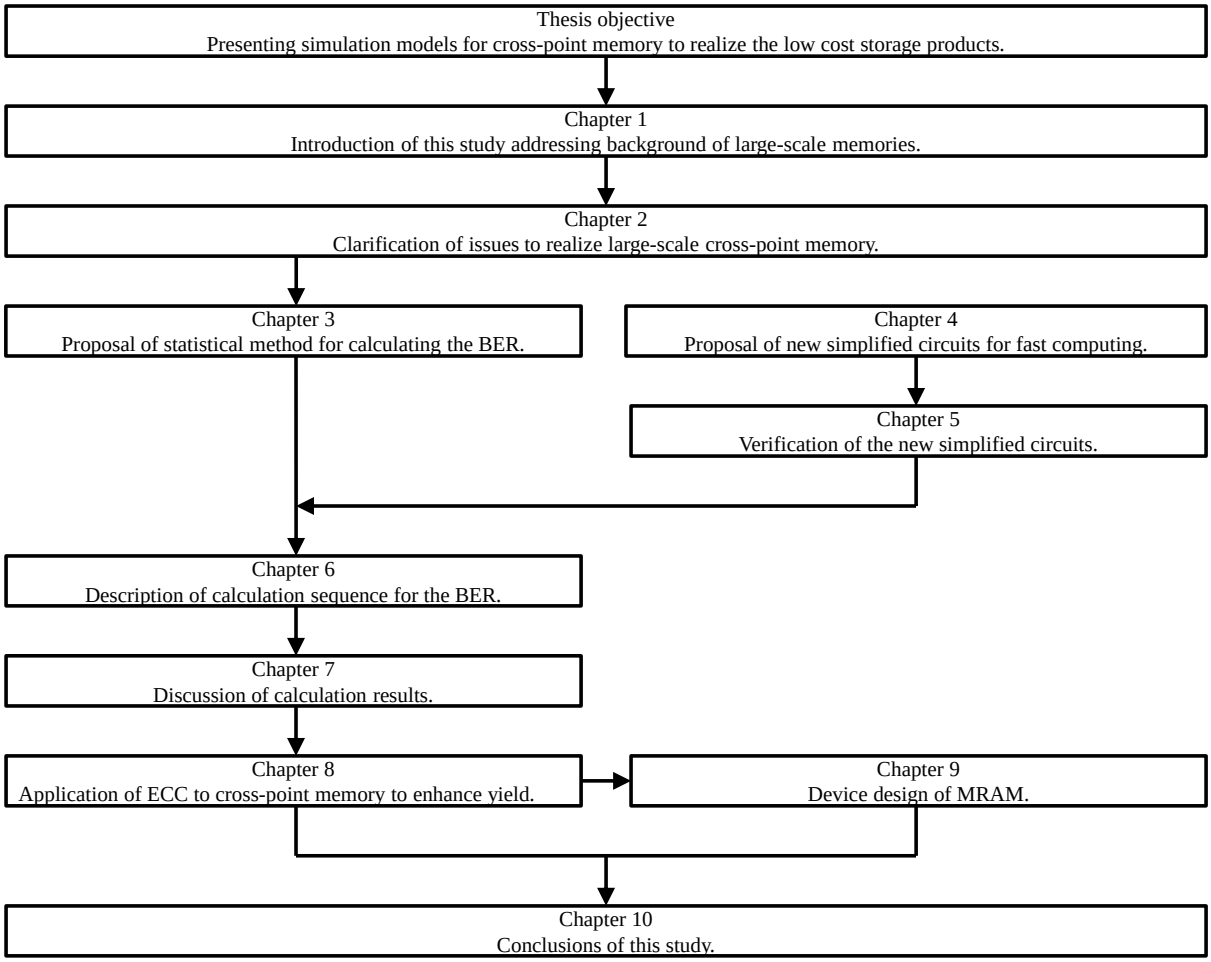


Fig. 1.6 Organization of this study.

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Chapter 2 Issues to realize large-scale cross-point memory

2.1 Organization of Chapter 2

This chapter reviews the issues associated with the realization of large-scale cross-point memory. As disturbances occur during read and write cycles in the cross-point array, there is a trade-off relationship between the disturbance and the write error. This limits the yield of the cross-point memory. In addition, it is difficult to estimate the yield because it takes a long time to calculate the cell current flowing through the cross-point array. This section is organized as follows.

After explaining the ReRAM cell structure in Section 2.2, an equivalent circuit is explained in Section 2.3 and a numerical solution for the electrical current flowing through the cross-point array is introduced in Section 2.4. As discussed in Chapter 1, it takes a long time to calculate the electrical current. This is demonstrated in Section 2.5. In Section 2.6, failures in the cross-point array are reviewed. They depend on the voltage applied on the non-selected metal wires. Finally, in Section 2.7, this chapter concludes by summarizing the issues associated with realizing large-scale cross-point memory.

2.2 ReRAM cell structure

As the memory cell of ReRAM has two terminals, it is suitable for a cross-point array. The memory cell is composed of two orthogonal metal wires and a memory element, as shown in Fig. 2.1. The memory element includes a diode. Let the upper and lower metal wires be a word-line (WL) and a bit-line (BL), respectively. ReRAM has the potential to offer large-scale memory because the unit cell size is $4F^2$, where F is the feature size, and because 3D memory arrays are possible.

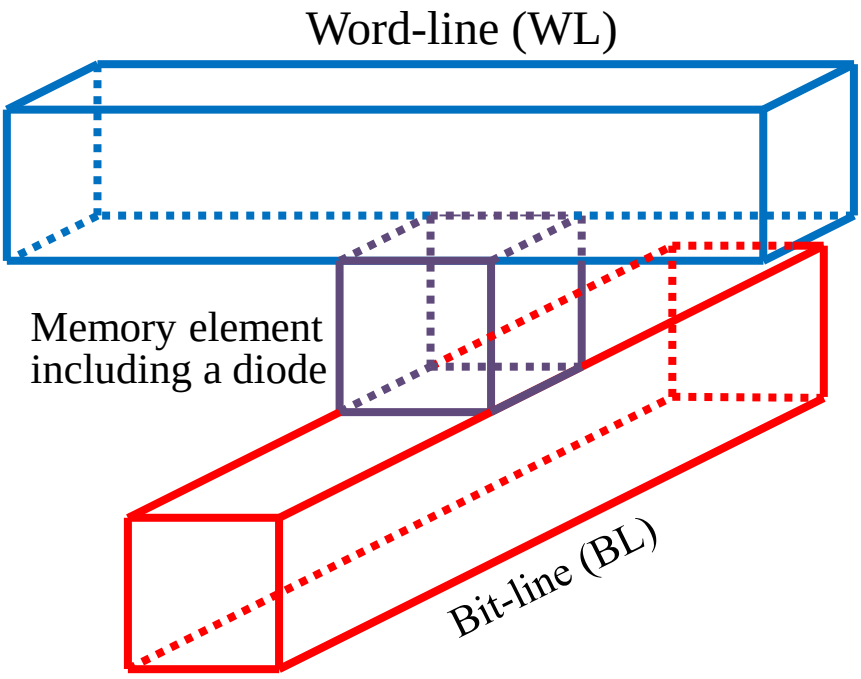


Fig. 2.1 ReRAM cell structure [24].

2.3 Equivalent circuit of cross-point array

Suppose that a cross-point array is composed of m WLs, n BLs, and $m \times n$ memory elements, as shown in Fig. 2.2 [23]. The upper-left corner is defined as the origin. Here, the address is written as (i, j) for $i = 1, 2, \cdots, m$ and $j = 1, 2, \cdots, n$.

An equivalent circuit of the cross-point array is illustrated in Fig. 2.3 [23], where each cell is composed of WL resistance $r_{\mathrm{WL}k}$, BL resistance $r_{\mathrm{BL}k}$, and memory element resistance $r_{\mathrm{M}k}$ for $k = 1, 2, \cdots, mn$. At the periphery of the array, the voltage sources $V_{\mathrm{WL}i}$ and $V_{\mathrm{BL}j}$ are connected to WL_i and BL_j, respectively. By applying the appropriate voltage to the voltage sources, read and write operations can be conducted.

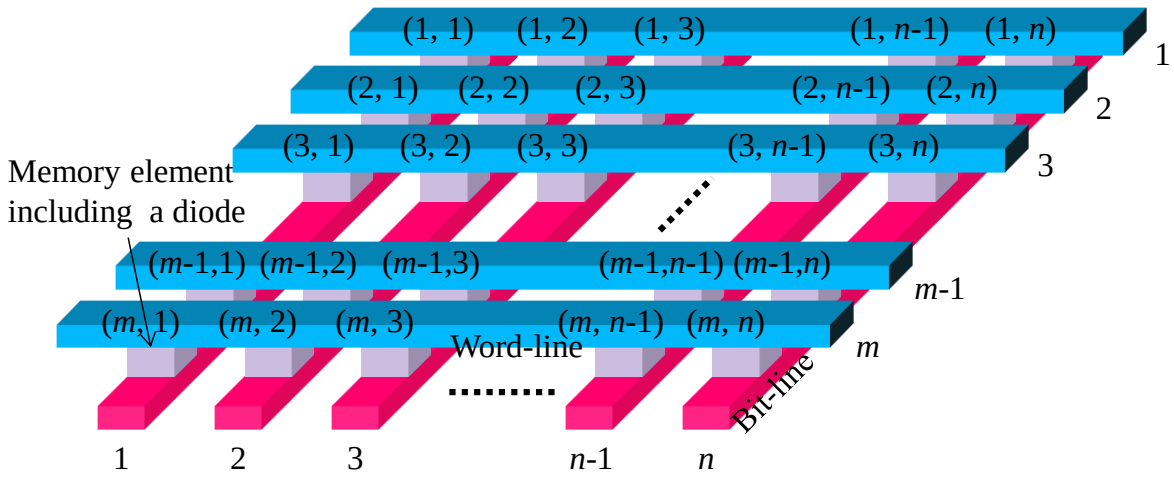


Fig. 2.2 Schematic view of cross-point array [23][24].

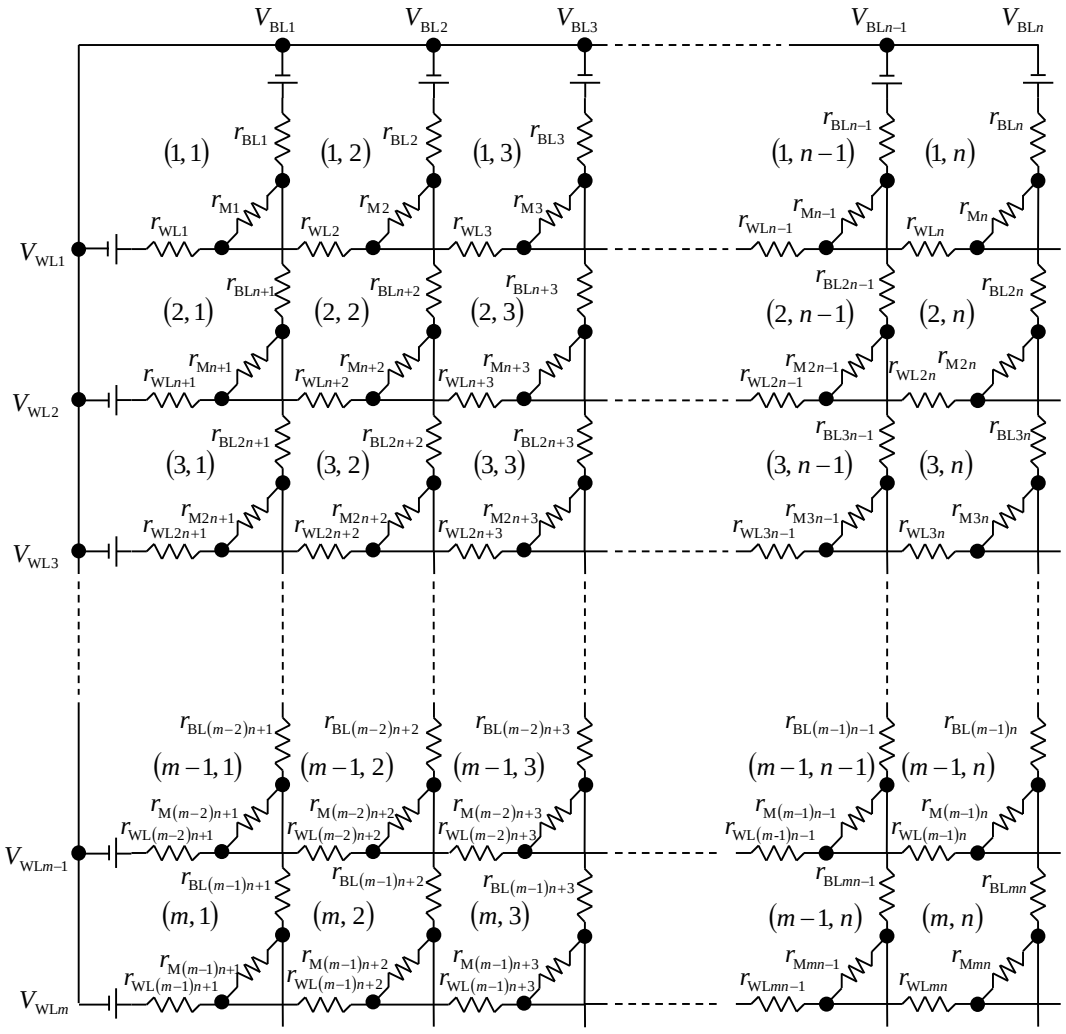


Fig. 2.3 Equivalent circuit of cross-point array [23][24].

2.4 Numerical solution of electric current flowing through cross-point array

In this section, a numerical solution is introduced for the electric current flowing through the cross-point array. As the equivalent circuit in Fig. 2.3 includes only linear resistive elements, the current can be derived using simultaneous linear equations. After introducing the simultaneous linear equations in this section, the calculation time is demonstrated for several computational methods in the next section. The consequent dependence of the mat size on the failure rate is discussed in Section 7.1.

Kirchhoff's laws are applied to the equivalent circuit in Fig. 2.3 to calculate the current. As the first step in Kirchhoff's laws, a closed loop current i_k is assigned for k = 1, 2, ⋯, mn, as shown in Fig. 2.4 [23]. The subscript k is given by the address (i, j) as

$$k = (i-1)n + j \qquad \text{Eq. 2.1}$$

for i = 1, 2, ⋯, m and for j = 1, 2, ⋯, n. The voltage drop v_k along the closed loop current i_k is expressed as

$$\begin{aligned} v_k = {} & r_{\mathrm{M}k}(i_k - i_{k+1} - i_{k+n} + i_{k+n+1}) \\ & + r_{\mathrm{WL}k}(i_k - i_{k+n}) \\ & + r_{\mathrm{M}k-1}(-i_{k-1} + i_k + i_{k+n-1} - i_{k+n}) \\ & + r_{\mathrm{BL}k-1}(-i_{k-1} + i_k) \\ & + r_{\mathrm{M}k-n-1}(i_{k-n-1} - i_{k-n} - i_{k-1} + i_k) \\ & + r_{\mathrm{WL}k-1}(-i_{k-n} + i_k) \\ & + r_{\mathrm{M}k-n}(-i_{k-n} + i_{k-n+1} + i_k - i_{k+1}) \\ & + r_{\mathrm{BL}k}(i_k - i_{k+1}) \end{aligned} \qquad \text{Eq. 2.2}$$

for k = 1, 2, ⋯, mn [23]. The following equation can be obtained by rearranging Eq. 2.2:

$$\begin{aligned} v_k = {} & r_{\mathrm{M}k-n-1} i_{k-n-1} \\ & - (r_{\mathrm{M}k-n-1} + r_{\mathrm{M}k-n} + r_{\mathrm{WL}k-n}) i_{k-n} \\ & + r_{\mathrm{M}k-n} i_{k-n+1} \\ & - (r_{\mathrm{M}k-n-1} + r_{\mathrm{M}k-1} + r_{\mathrm{BL}k-1}) i_{k-1} \\ & + (r_{\mathrm{M}k-n-1} + r_{\mathrm{M}k-n} + r_{\mathrm{WL}k-n} + r_{\mathrm{M}k-1} + r_{\mathrm{BL}k-1} + r_{\mathrm{M}k} + r_{\mathrm{WL}k} + r_{\mathrm{BL}k}) i_k \\ & - (r_{\mathrm{M}k-n} + r_{\mathrm{M}k} + r_{\mathrm{BL}k}) i_{k+1} \\ & + r_{\mathrm{M}k-1} i_{k+n-1} \\ & - (r_{\mathrm{M}k-1} + r_{\mathrm{M}k} + r_{\mathrm{WL}k}) i_{k+n} \\ & + r_{\mathrm{M}k} i_{k+n+1}. \end{aligned} \qquad \text{Eq. 2.3}$$

Consequently, the simultaneous linear equations of degree $m \times n$ are derived as

$$\begin{pmatrix} v_1 \\ v_2 \\ \vdots \\ v_{mn} \end{pmatrix} = \begin{pmatrix} a_{11} & a_{12} & \cdots & a_{1mn} \\ a_{21} & a_{22} & \cdots & a_{2mn} \\ & & \cdots & \\ a_{mn1} & a_{mn2} & \cdots & a_{mnmn} \end{pmatrix} \begin{pmatrix} i_1 \\ i_2 \\ \vdots \\ i_{mn} \end{pmatrix}, \quad \text{Eq. 2.4}$$

where the elements of the coefficient matrix a_{xy} are given by

$$a_{xy} = \begin{cases} r_{\mathrm{M}x-n-1} & \text{if } y = x-n-1, \\ -r_{\mathrm{M}x-n-1} - r_{\mathrm{M}x-n} - r_{\mathrm{WL}x-n} & \text{if } y = x-n, \\ r_{\mathrm{M}x-n} & \text{if } y = x-n+1, \\ -r_{\mathrm{M}x-n-1} - r_{\mathrm{M}x-1} - r_{\mathrm{BL}x-1} & \text{if } y = x-1, \\ \sum_{d=0}^{1} \left(\sum_{e=0}^{1} r_{\mathrm{M}x-ne-b} + r_{\mathrm{WL}x-nb} + r_{\mathrm{BL}x-b} \right) & \text{if } y = x, \\ -r_{\mathrm{M}x-n} - r_{\mathrm{M}x} - r_{\mathrm{BL}x} & \text{if } y = x+1, \\ r_{\mathrm{M}x-1} & \text{if } y = x+n-1, \\ -r_{\mathrm{M}x-1} - r_{\mathrm{M}x} - r_{\mathrm{WL}x} & \text{if } y = x+n, \\ r_{\mathrm{M}x} & \text{if } y = x+n+1, \\ 0 & \text{otherwise,} \end{cases} \quad \text{Eq. 2.5}$$

for $x = 1, 2, \cdots, mn$ and $y = 1, 2, \cdots, mn$ [23]. The constant term v_k is given by

$$v_k = \begin{cases} V_{\mathrm{BL}1} - V_{\mathrm{WL}1} & \text{if } k = 1, \\ V_{\mathrm{BL}k} - V_{\mathrm{BL}k-1} & \text{if } 2 \le k \le n, \\ V_{\mathrm{WL}(k-1)/n} - V_{\mathrm{WL}(k-1)/n+1} & \text{if } k = n+1, \cdots, (m-1)n+1, \\ 0 & \text{otherwise,} \end{cases} \quad \text{Eq. 2.6}$$

for $k = 1, 2, \cdots, mn$ [23]. Consequently, the current can be obtained by solving Eq. 2.4 for i_k.

There are several calculation methods to solve simultaneous linear equations, namely, Gauss elimination, LU decomposition, and Cholesky decomposition [25]. In those, Gauss elimination succeeded in verifying the simultaneous linear equations in Eq. 4.2 by comparing the calculation result using SPICE. These two methods agreed with 15 significant digits. The program was coded in C and executed on a computer with 4 GB DRAM and a 3.4 GHz processor.

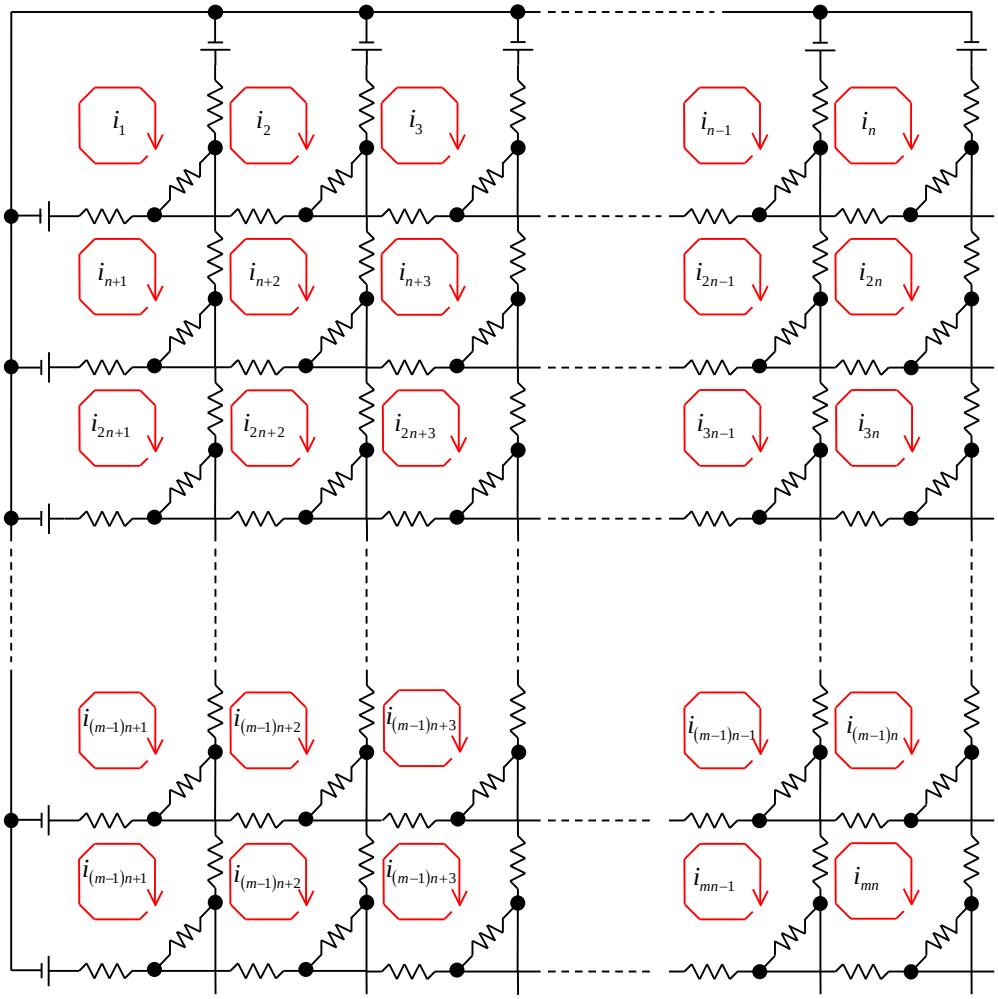


Fig. 2.4 Assignment of closed loops [23][24].

2.5 Calculation time for solving current equations in the cross-point array

In this section, the simultaneous linear equations are solved to demonstrate the time required to calculate the current in the cross-point array. As mentioned previously, these calculations take a long time when the mat size $m \times n$ is large. The dependence of the mat size on the calculation time is demonstrated to reveal that the calculation does not finish within a realistic time in the case of the mat size used for large-scale products.

The calculation time of the current in the cross-point array is illustrated in Fig. 2.5, where the approximated line is given by $3.22 \times 10^{-9} \times (mn)^{2.07}$. The number of WLs is the same

as that of BLs, i.e., $m = n$. The program was coded in C and executed on a computer with 4 GB DRAM and a 3.4 GHz processor. The calculation method used the Cholesky decomposition [25]. When $m = n = 4096$, the calculation time is 2,904,197 s (more than 33 days). Thus, the current in large-scale cross-point arrays cannot be computed within a realistic time.

As will be discussed in Chapter 3, the BERs can be obtained by repeating the calculations illustrated in Fig. 2.5, but the calculations do not finish within a practical time. Therefore, in this study simplified circuits are developed for the fast computation of the current. The circuits are described in Chapter 4.

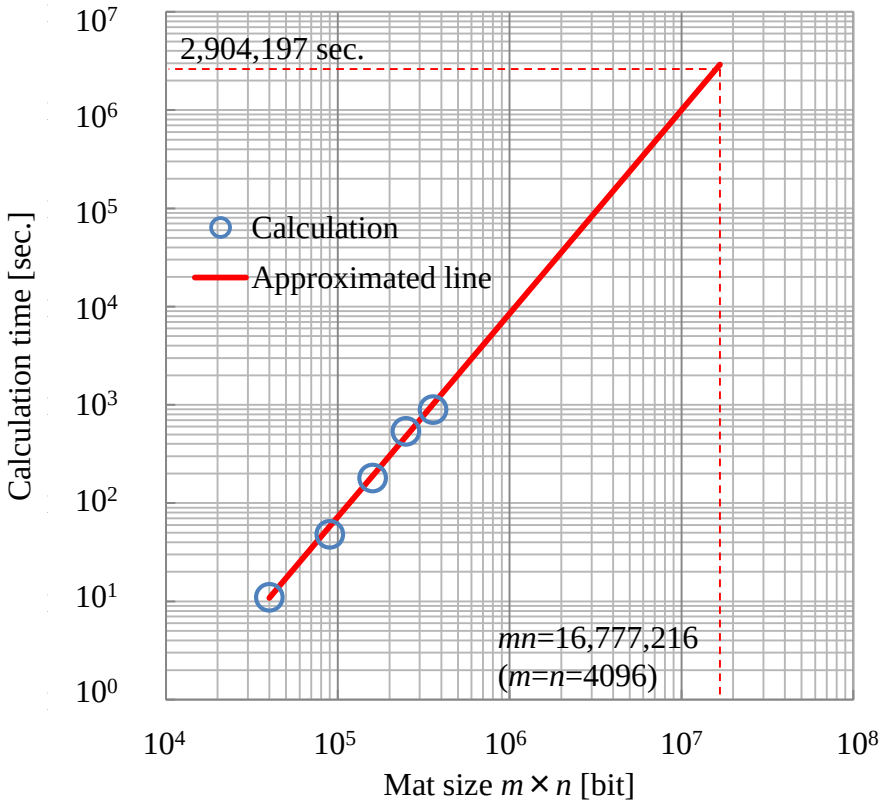


Fig. 2.5 Calculation time of the current in the cross-point array [23].

2.6 Unipolar and bipolar writing memories

In this section, several predictable failures in the cross-point array are reviewed. There is a difference in bias schemes between unipolar and bipolar writing memories. In unipolar writing memory, data are written by applying a current on the memory element in one direction. Bipolar writing memory allows data to be written by applying a current on the memory element in two directions. The V_{DD} scheme is used for unipolar writing memory, as shown in Fig. 2.6 [24]. A diode is clearly shown in the unit cell of the unipolar writing memory because the cell current flows in one direction. In contrast, bipolar writing memory uses the $V_{DD}/2$ and the $V_{DD}/3$ schemes, as shown in Figs. 2.7 and 2.8, respectively [24]. A bi-directional diode is inserted in the bipolar writing memory because the cell current flows in two directions.

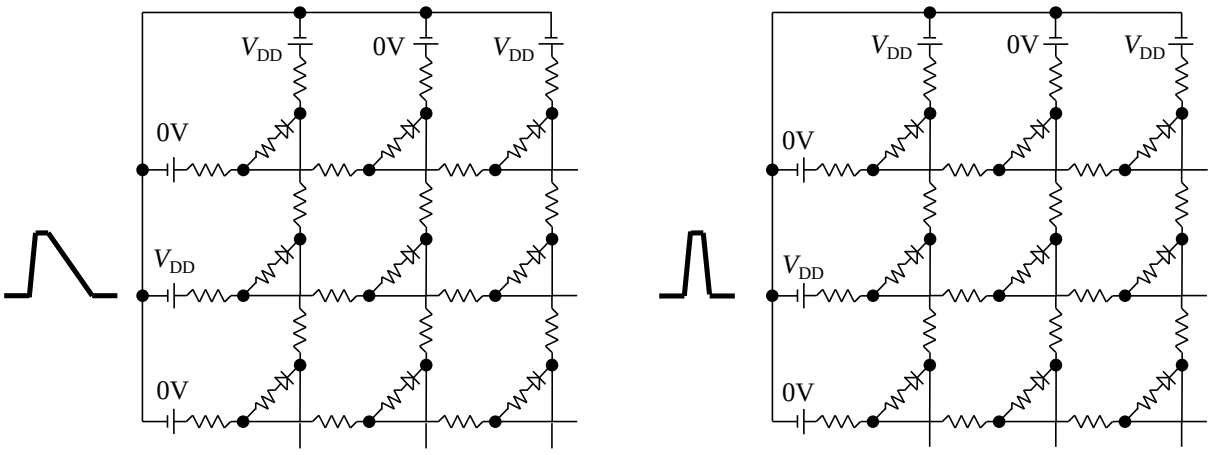
In unipolar writing memory, no bias is applied to the half-selected addresses, whereas V_{DD} is applied to the selected one. Therefore, no disturbance can occur in the half-selected or non-selected addresses. In bipolar writing memory with the $V_{DD}/2$ scheme, $V_{DD}/2$ is applied to the half-selected addresses, whereas V_{DD} is applied to the selected one. Therefore, a disturbance may occur in the half-selected addresses. However, no disturbance can occur in the non-selected addresses, because no bias is applied to them.

If the $V_{DD}/3$ scheme is used for bipolar writing memory, $V_{DD}/3$ will be applied to the half-selected addresses. Thus, the half-selected disturbance with the $V_{DD}/3$ scheme is less than that with the $V_{DD}/2$ scheme. However, the $V_{DD}/3$ scheme suffers the side-effect of non-selected disturbance. As $V_{DD}/3$ is applied to the non-selected addresses in a reverse bias, non-selected disturbances may occur.

The approximated *I-V* curves of the unipolar and bipolar writing memories are shown in Fig. 2.9 (a) and (b), respectively [24]. It is assumed that the resistance of the memory element is independent of the applied voltage.

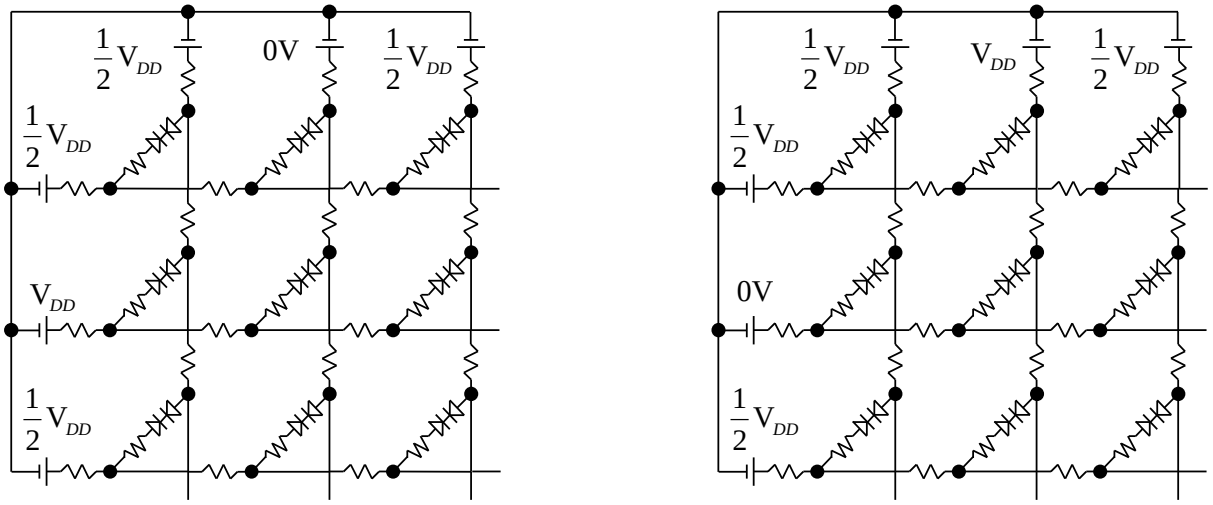
Table 2.1 summarizes the predictable failures in the write operation [24]. The voltage applied to the memory element is given in parentheses, where r_{WL} and r_{BL} are neglected. The trade-off relationship between the disturbance and the write error is illustrated in Fig. 2.10 [23]. Each memory element in the cross-point array has a switching threshold current (I_{TH}), read current (I_{READ}), half-selected current by a WL or a BL (I_{HALF}), non-selected current (I_{NON}), and write current (I_{WRITE}). If I_{TH} is greater than I_{WRITE} for a certain cell, the cell suffers a write error. Similarly, if I_{TH} is less than I_{READ}, I_{HALF}, or I_{NON}, the cell suffers a read disturbance for the selected address, write disturbance for the half-selected address, or write disturbance for the non-selected address, respectively.

These currents are distributed across an array according to process deviations and the metal wire length determined by the address. Consequently, their frequency curves are designed not to induce disturbances and write errors, as illustrated in Fig. 2.10, where two guard bands are inserted for the disturbance and the write error. To prevent the disturbance, I_{CELL} is set to be less than I_{TH}, where I_{READ}, I_{HALF}, and I_{NON} are simply denoted by I_{CELL}. Simultaneously, to prevent write errors, I_{WRITE} is set to be greater than I_{TH}. If the guard bands are too small, failures will occur.



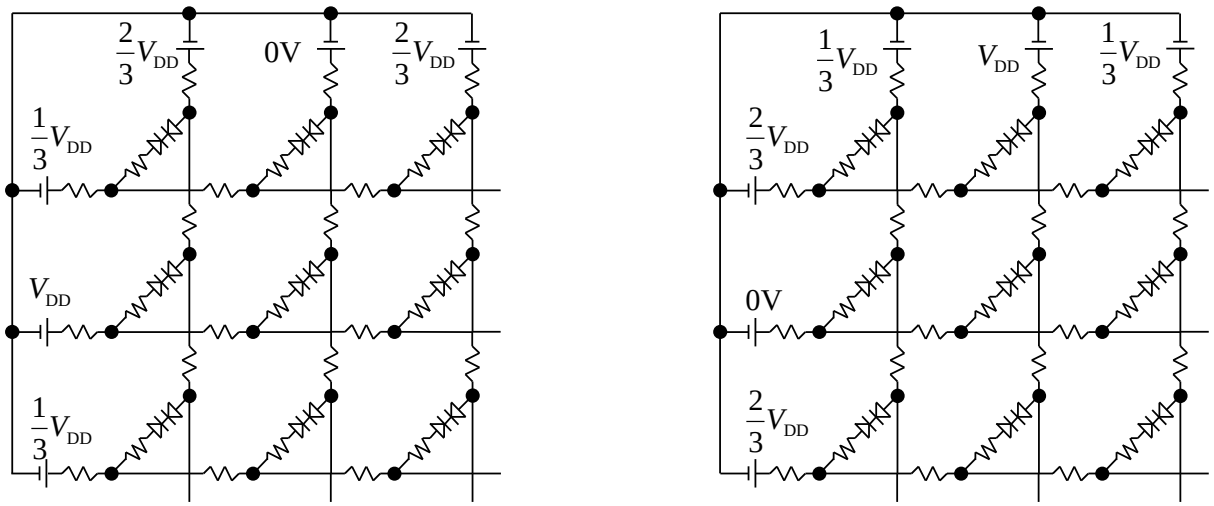
(a) SET operation. (b) RESET operation

Fig. 2.6 V_{DD} bias schemes for unipolar writing memory [24]. The center cell is selected in each circuit. In the SET[21] operation (a), a long-tail pulse is applied to crystalize the memory element $Ge_2Sb_2Te_5$ in PCM. In the RESET[22] operation (b), a short-tail pulse is applied to make the memory material $Ge_2Sb_2Te_5$ amorphous [12].



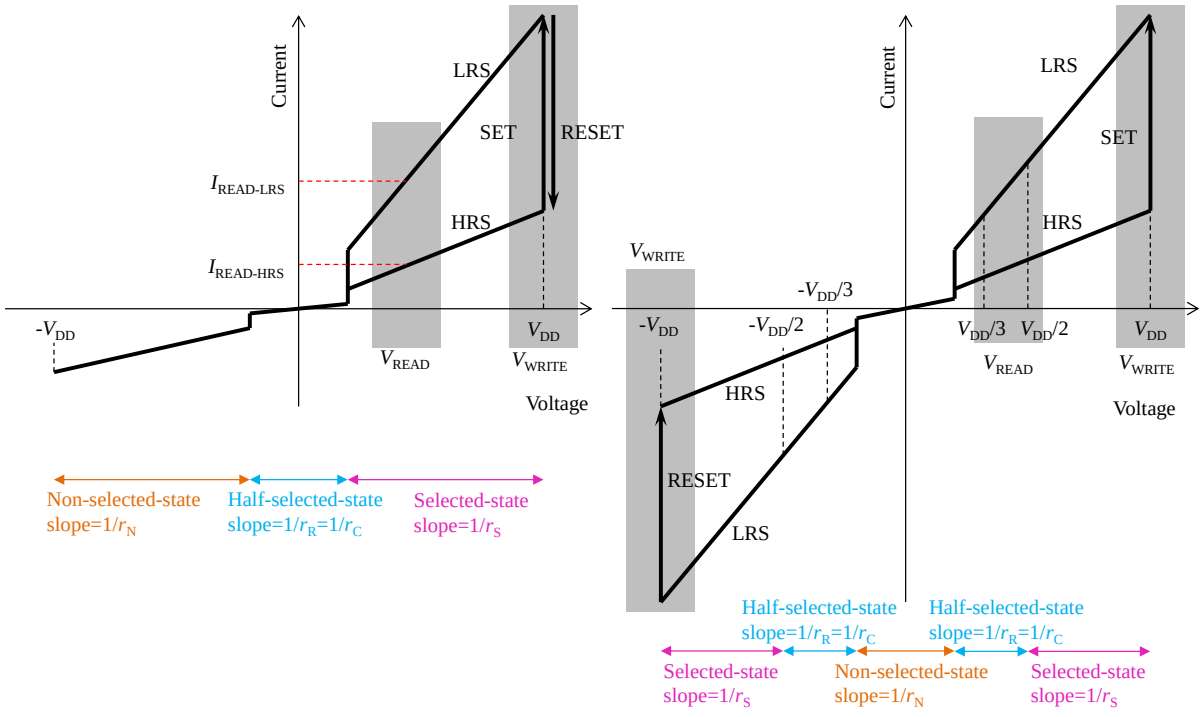
(a) SET operation. (b) RESET operation.

Fig. 2.7 $V_{DD}/2$ bias scheme for bipolar writing memory [24].



(a) SET operation. (b) RESET operation.

Fig. 2.8 $V_{DD}/3$ bias scheme for bipolar writing memory [24].



(a) Unipolar writing memory. (b) Bipolar writing memory.

Fig. 2.9 *I-V* curves of memory element [23][24].

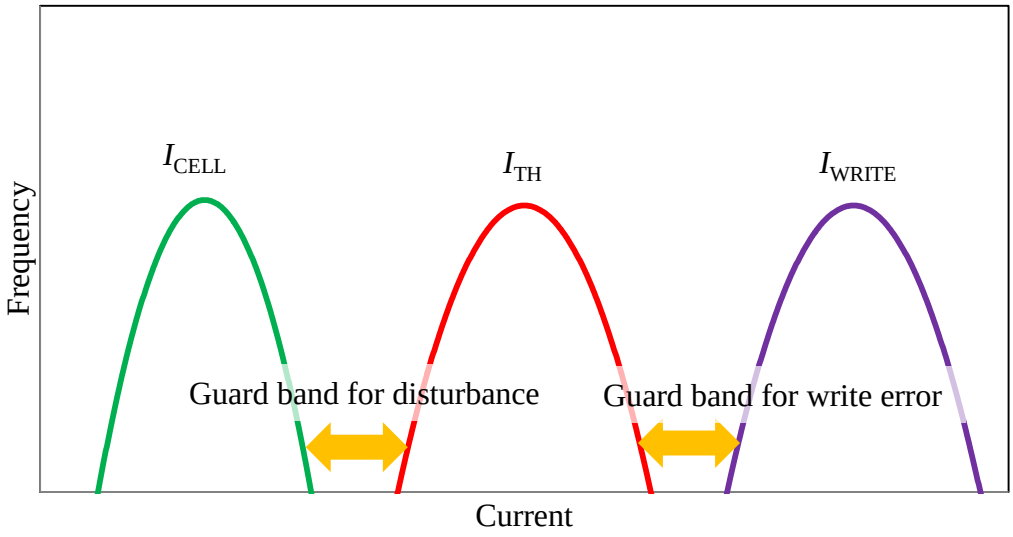


Fig. 2.10 Frequency curves of cell, switching threshold, and write currents [23][24].

Table 2.1 Predictable failures in the cross-point array [24].

	Unipolar V_{DD} scheme	Bipolar $V_{DD}/2$ scheme	$V_{DD}/3$ scheme
Selected cell	Read disturbance Write error (V_{DD})	Read disturbance Write error (V_{DD})	Read disturbance Write error (V_{DD})
Half-selected cell	N/A (0V)	Write Disturbance ($V_{DD}/2$)	Write disturbance ($V_{DD}/3$)
Non-selected cell	N/A ($-V_{DD}$)	N/A (0V)	Write disturbance ($-V_{DD}/3$)

2.7 Summary

Two issues associated with the realization of large-scale cross-point memory have been reviewed. The first is the trade-off relationship between the disturbance and the write error, and the second is the long calculation time of the cell current in a cross-point array, which is needed to estimate the BER due to the trade-off relationship. To solve these problems, a fast computation technique for the cell current in the cross-point array is required to enable the design of large-scale cross-point memory.

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Chapter 3 Estimation of bit error rate

3.1 Bit error rate caused by disturbance and write error

As described in Chapter 2, one of the issues in realizing large-scale cross-point memory is the trade-off relationship between the disturbance and the write error. The disturbance and the write error are induced by fluctuations in the switching threshold current I_{TH} and the cell current I_{CELL}. The fluctuations are caused by process deviations and by the metal wire length, which depends on the address. In this chapter, a statistical solution for the BERs caused by the disturbance and the write error is introduced. This solution is developed using the two-dimensional probability density function.

As summarized in Table 2.1, there are two types of disturbance, namely read and write disturbances. The former occurs in the selected address during the read cycle, whereas the latter occur in the half-selected and non-selected addresses during the write cycle. Write errors only occur in the selected address during the write cycle. Thus, two trade-offs are possible: that between the read disturbance and write error, and that between the write disturbance and write error.

The BER caused by disturbances and write errors can be calculated using a two-dimensional probability density function. The calculation algorithm is based on a comparison of I_{TH} with I_{CELL}. Details are explained in Section 3.2.

3.2 Bit error rate solution with two-dimensional probability density function

Each memory element in a cross-point array has its own switching threshold current I_{TH} and cell current I_{CELL}. These currents are distributed across the array, and can be expressed by a two-dimensional function. Let $f(x, y)$ be the joint probability density function of the switching threshold current x and the cell current y. If these currents obey the normal distribution, $f(x, y)$

is given by the bivariate normal distribution

$$f(x,y) = \frac{1}{2\pi\sigma_x\sigma_y\sqrt{1-\rho^2}} \mathrm{e}^{-\frac{1}{2(1-\rho^2)}\left[\frac{(x-\mu_x)^2}{\sigma_x^2} - \frac{2\rho(x-\mu_x)(y-\mu_y)}{\sigma_x\sigma_y} + \frac{(y-\mu_y)^2}{\sigma_y^2}\right]}, \quad \text{Eq. 3.1}$$

where μ_x, σ_x, μ_y, σ_y, and ρ denote the expectation of x, standard deviation of x, expectation of y, standard deviation of y, and correlation coefficient of x and y, respectively. An example of the distribution curve is shown in Fig. 3.1, where $\mu_x = \mu_y = 1$, $\sigma_x = \sigma_y = 0.2$, and $\rho = 0$.

If the cell current y exceeds the switching threshold current x, a disturbance occurs. By integrating over the region in which x is larger than y, the disturbance probability F_{DISTURB} can be obtained as [23][24][26]

$$F_{\mathrm{DISTURB}} = \int_0^{\infty}\int_0^{y} f(x,y)dxdy. \quad \text{Eq. 3.2}$$

The contour map of $f(x, y)$ is illustrated in Fig. 3.2. The shaded region of Fig. 3.2 (a) is integrated in Eq. 3.2.

In the same manner, if the cell current y is less than the switching threshold current x, a write error occurs. The write error probability F_{WRITE} is expressed by [23][24][26]

$$F_{\mathrm{WRITE}} = \int_0^{\infty}\int_y^{\infty} f(x,y)dxdy. \quad \text{Eq. 3.3}$$

The shaded region of Fig. 3.2 (b) is integrated in Eq. 3.3.

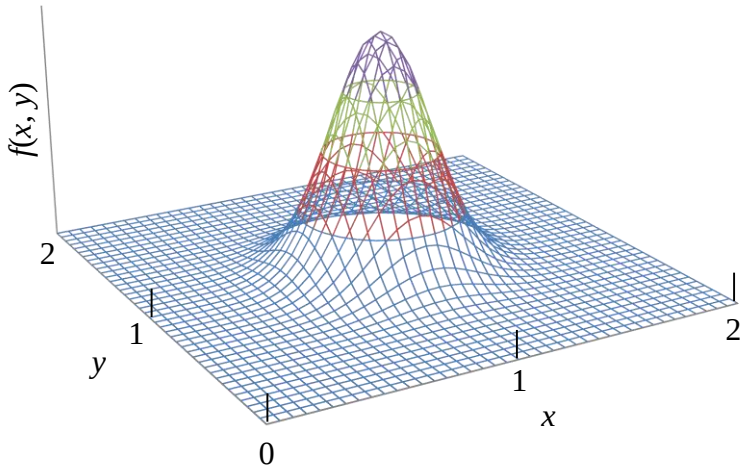
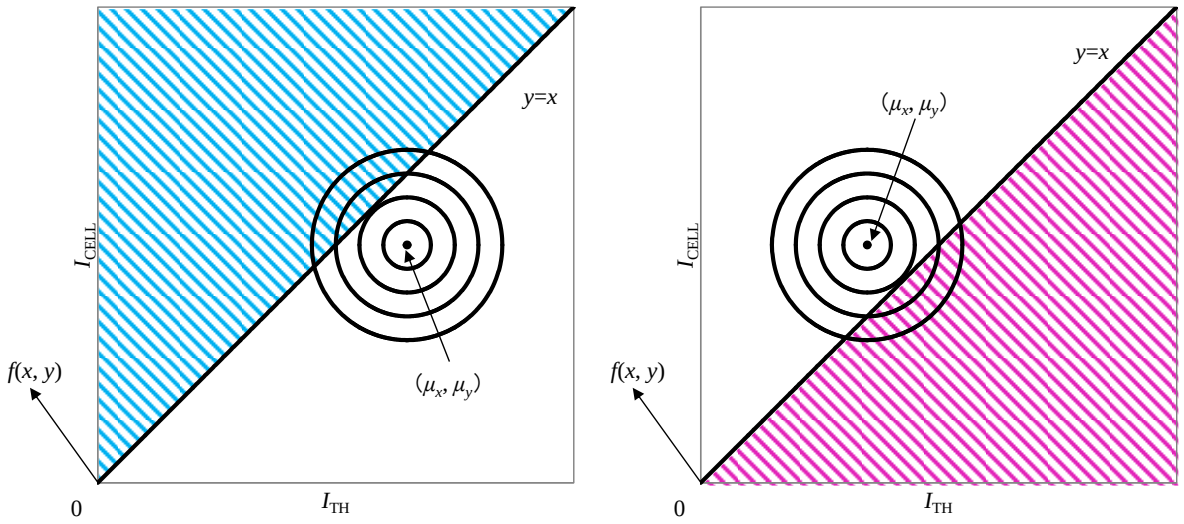


Fig. 3.1 Bivariate normal distribution curve, where $\mu_x = \mu_y = 1$, $\sigma_x = \sigma_y = 0.2$, and $\rho = 0$ [23].



(a) Disturbance

(b) Write error

Fig. 3.2 Contour maps of the bivariate normal distribution and regions of integration [23][24].

3.3 Summary

The numerical solution of the BER caused by disturbances and write errors has been introduced using the two-dimensional probability density function. The algorithm is based on a comparison of the threshold current I_{TH} with the cell current I_{CELL}. The distributions of I_{TH} and I_{CELL} are a result of process deviations and the selected address. The solution takes the deviation current into account, and then, it represents a comprehensive tool for optimizing the BER.

References

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Chapter 4 Fast computation of cell current using advanced simplified circuits

4.1 Conventional simplified circuit and its limitation

4.1.1 Concept of simplified circuit

As proved in Section 2.5, it takes a long time to calculate the cell current flowing through the cross-point array when the mat size is large, and then, several simplified circuits have been developed to enable fast calculations of the cell current [27][28][29][30][31]. In this section, the conventional simplified circuit is introduced.

The conventional simplified circuit is illustrated in Fig. 4.1 [23][24][30]. This is a modified version of the original circuit in Fig. 2.3, where the mat size is $m \times n$. The conventional simplified circuit in Fig. 4.1 has two WLs, two BLs, and four memory elements. Here, r_{WL} and r_{BL} are defined as the resistances of a WL and a BL between the two adjacent cells of the original circuit in Fig. 2.3, respectively. Similarly, let r_R, r_C, r_N, and r_S be the resistances of the half-selected cell by the WL, the half-selected cell by the BL, the non-selected cell, and the selected cell, respectively.

Note that a sneak current flows in the cross-point array, as indicated in Fig. 4.2. This sneak current is generated by leakage from the diodes at the half-selected and non-selected cells. If the sneak current is sufficiently high, the read and write currents supplied by a voltage source will not reach the selected cells. Therefore, the conventional simplified circuit approximates the sneak current path using three resistors, r_R, r_N, and r_C.

The relationship between the original and the conventional simplified circuits is clarified in Fig. 4.3 [23]. The lower right cell in Fig. 4.1 is the selected cell, which is the farthest from the voltage sources V_{WL2} and V_{BL2}. This cell consists of one resistor with resistance r_S, one WL with resistance $nr_{WL}/2$, and one BL with resistance $mr_{BL}/2$. The resistances $nr_{WL}/2$ and $mr_{BL}/2$ correspond to half of the total WL and BL resistances, respectively.

The lower left cell of Fig. 4.1 represents $n-1$ half-selected cells by WL in parallel. This cell consists of one resistor with resistance $r_R/(n-1)$, one WL with resistance $nr_{WL}/2$, and one BL with resistance $mr_{BL}/[2(n-1)]$. The resistances $nr_{WL}/2$ and $mr_{BL}/[2(n-1)]$ correspond to half of one WL and $n-1$ BL resistances in parallel, respectively.

In the same manner, the upper right cell of Fig. 4.1 represents $m-1$ half-selected cells by BL in parallel. This cell consists of one resistor with resistance $r_C/(m-1)$, one WL with resistance $nr_{WL}/[2(m-1)]$, and one BL with resistance $mr_{BL}/2$. The resistances $nr_{WL}/2$ and $mr_{BL}/2$ correspond to half of the $m-1$ WLs in parallel and one BL resistance, respectively.

Finally, the upper left cell of Fig. 4.1 represents $(m-1)(n-1)$ non-selected cells in parallel. This cell consists of one resistor with resistance $r_N/[(m-1)(n-1)]$, one WL with resistance $nr_{WL}/[2(m-1)]$, and one BL with resistance $mr_{BL}/[2(n-1)]$. The resistances $nr_{WL}/[2(m-1)]$ and $mr_{BL}/[2(n-1)]$ correspond to half of the $m-1$ WL and $n-1$ BL resistances in parallel, respectively.

The fundamental idea of the conventional simplified circuit in Fig. 4.1 is that the wire resistance is the main BER limiter of the write error. This is because the lower right cell has the longest wire length among the cross-point array cells. Accordingly, the conventional simplified circuit is designed to estimate the worst-case write error caused by wire resistance.

However, the conventional simplified circuit is not applicable to cases where the wire resistance is low and the memory element resistance is the main BER limiter of write errors. The effect of the wire resistance deviation will be analyzed in the next subsection. Furthermore, the conventional simplified circuit is not applicable to the analysis of read disturbances, because most disturbances occur in cells with low I_{TH}, as described in Fig. 2.10. Therefore, there are some difficulties in precisely estimating the BERs of read disturbances and write errors.

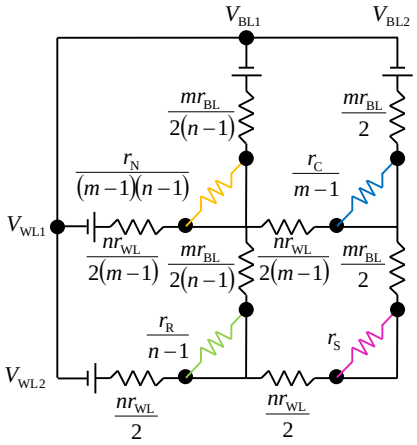


Fig. 4.1 Conventional simplified circuit [23][24].

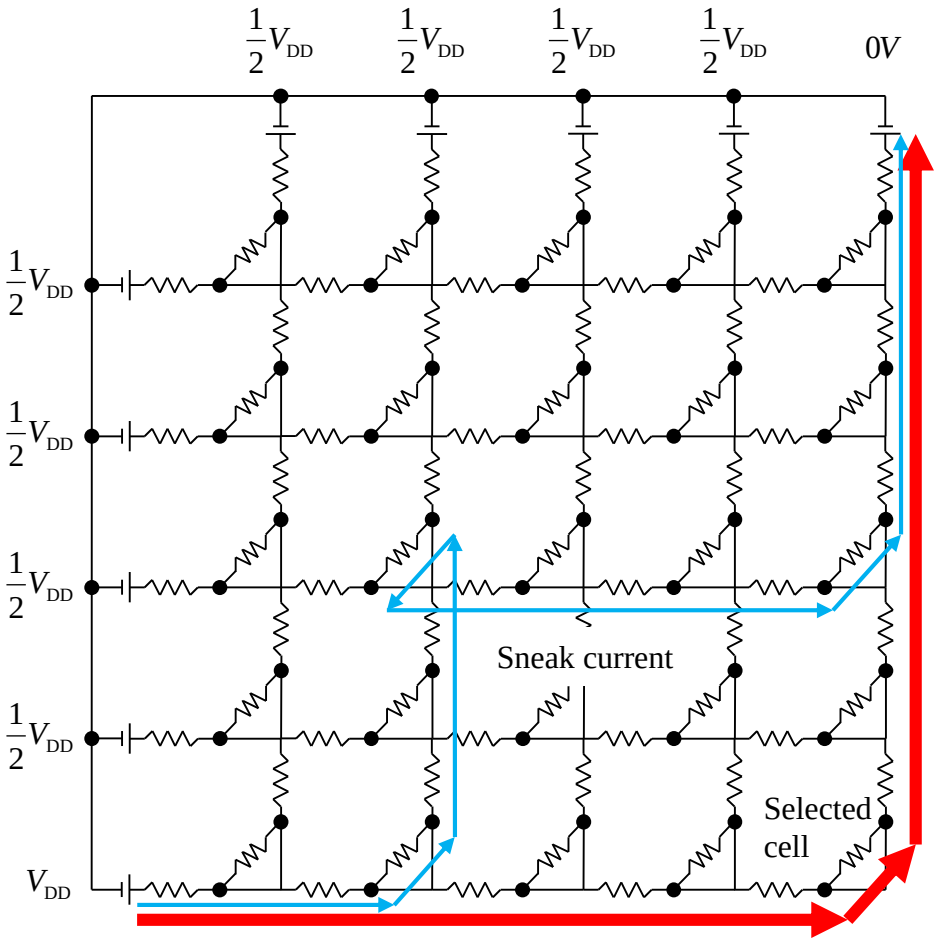
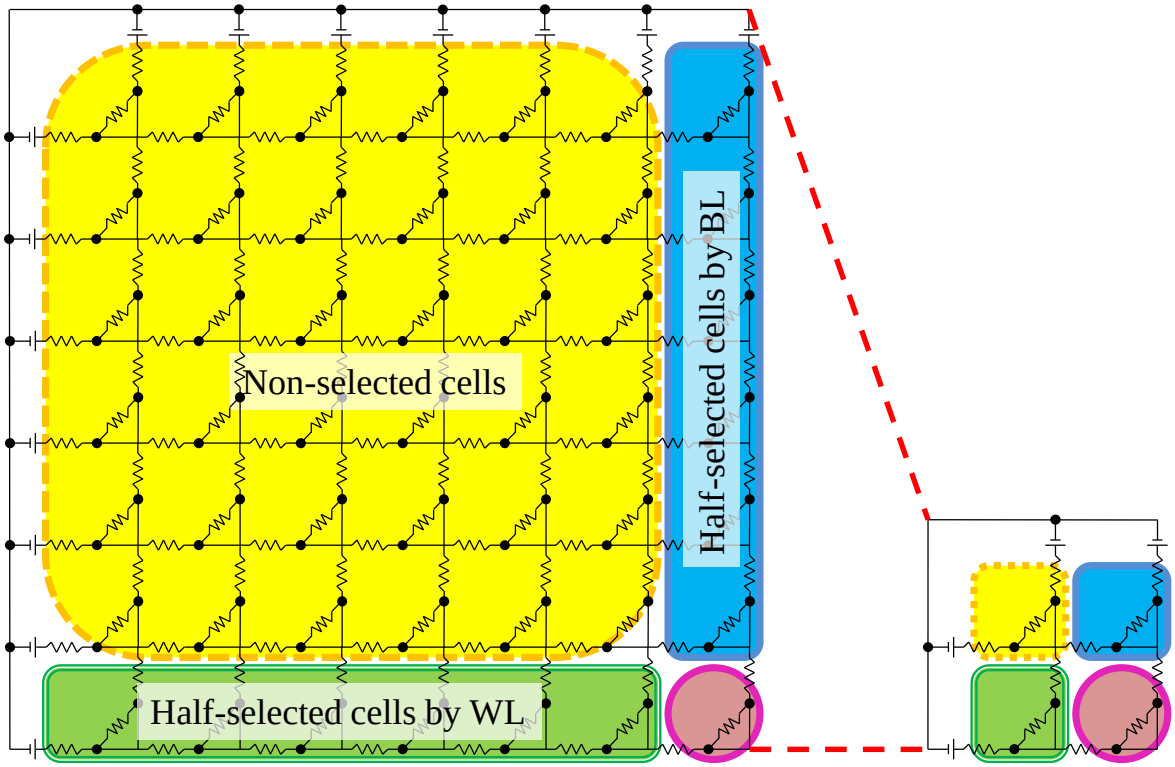


Fig. 4.2 Sneak current in cross-point array.



(a) Original circuit. (b) Simplified circuit.

Fig. 4.3 Relationship between original and conventional simplified circuits [23].

4.1.2 Current deviation caused by wire resistance varying with the selected address

Each memory element in the cross-point array has two parameters, I_{TH} and I_{CELL}. There are two major reasons why these are distributed across the array. The first is process deviation. The wire and the memory element are formed by deposition, lithography, and etching processes. As the condition of these processes fluctuates, the dimensions of the wire and the memory element will exhibit minor deviations. The second reason is the variation in wire length according to the memory address.

The relationship between I_{CELL} and the memory address is described below. It is assumed that the diode limits the reverse current in the cross-point array in Fig. 2.3. If address (x, y) is selected, the total resistance r_{total} is expressed as

$$r_{\text{total}} = xr_{\text{WL}} + yr_{\text{BL}} + r_{\text{CELL}}, \quad \text{Eq. 4.1}$$

where r_{WL}, r_{BL}, and r_{CELL} denote the WL, BL, and memory element resistances in the unit cell, respectively. Because r_{total} depends on the selected address, I_{CELL} has a distribution across the array. If the array size is $m \times n$, the expectation μ and standard deviation σ of r_{total} can be written as

$$\mu = \frac{1}{mn}\sum_{y=1}^{n}\sum_{x=1}^{m}(xr_{\text{WL}} + yr_{\text{BL}} + r_{\text{CELL}}), \quad \text{Eq. 4.2}$$

$$\sigma = \sqrt{\frac{1}{mn}\sum_{y=1}^{n}\sum_{x=1}^{m}(xr_{\text{WL}} + yr_{\text{BL}} + r_{\text{CELL}} - \mu)^2}, \quad \text{Eq. 4.3}$$

respectively. By the following expressions for the summation of an integer i and its square i^2

$$\sum_{i=1}^{N} i = \frac{N(N+1)}{2}, \quad \text{Eq. 4.4}$$

$$\sum_{i=1}^{N} i^2 = \frac{N(N+1)(2N+1)}{6}, \quad \text{Eq. 4.5}$$

Eqs. 4.6 and 4.7 become

$$\mu = \frac{1}{2}(m+1)r_{\text{WL}} + \frac{1}{2}(n+1)r_{\text{BL}} + r_{\text{CELL}}, \quad \text{Eq. 4.6}$$

$$\sigma = \sqrt{\begin{aligned}&\frac{1}{6}(m+1)(2m+1)r_{\text{WL}}^2 + \frac{1}{6}(n+1)(2n+1)r_{\text{BL}}^2 + \frac{1}{2}(m+1)(n+1)r_{\text{WL}}r_{\text{BL}} \\ &+ (r_{CELL} - \mu)[(m+1)r_{\text{WL}} + (n+1)r_{\text{BL}} + r_{CELL} - \mu]\end{aligned}}, \quad \text{Eq. 4.7}$$

respectively.

The standard deviation σ of the total resistance r_{total} is plotted in Fig. 4.4 as a function of the wire resistance normalized by the cell resistance. The parameter is the mat size $m \times n$, which ranges from 64×64 to 8192×8192, and r_{WL}, r_{BL} are assumed to have the same value. The standard deviation of r_{total} increases with the wire resistance and the mat size. This indicates that the switching threshold current I_{TH} must decrease as the mat size increases for write

operations. Therefore, the reduction of I_{TH} is an important factor in realizing a large-scale non-volatile memory. Figure 4.4 indicates that operation failure can be caused by higher wire resistance.

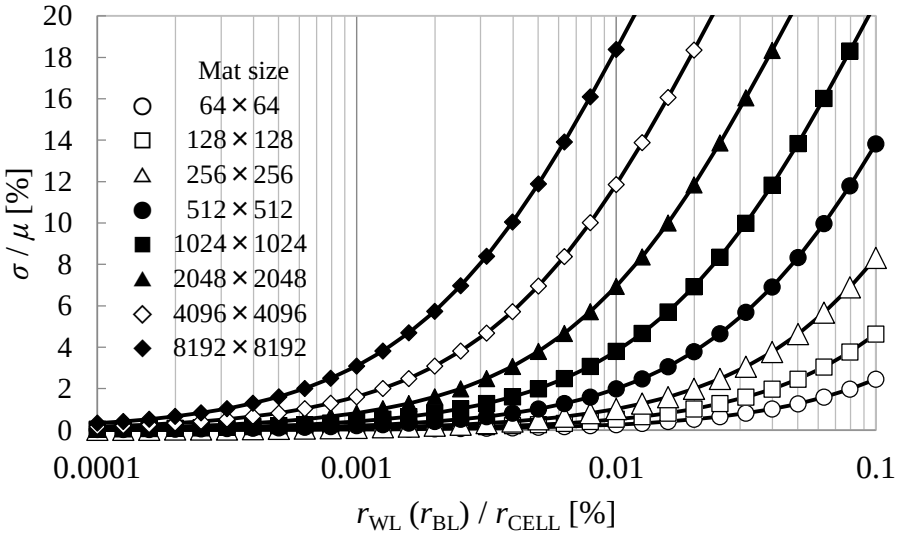


Fig. 4.4 Standard deviation of total resistance.

4.2 Proposal of advanced simplified circuits

4.2.1 Purpose of the proposed simplified circuits

Three simplified circuits are proposed in Subsections 4.2.2, 4.2.4, and 4.2.5. The first is designated to calculate the selected cell current. This circuit is expanded from the conventional simplified circuit in Fig. 4.1, and allows the read disturbance and the write error to be estimated. Details are described in Subsection 4.2.2. The second circuit (Subsection 4.2.4) is applicable to the estimation of the half-selected cell current. An additional cell is prepared in the simplified circuit for the half-selected cell, allowing the half-selected disturbance to be estimated. The third circuit (Subsection 4.2.5) approximates the non-selected cell current, giving the non-selected disturbance. Table 4.1 summarizes the simplified circuits and their targets.

Table 4.1 Simplified circuits and their targets

	Conventional Circuit	Proposed Circuit 1	Proposed Circuit 2	Proposed Circuit 3
Figure	Fig. 4.1	Fig. 4.5	Fig. 4.8	Fig. 4.14
Access cell	Selected cell at the corner address	Selected cell	Half-selected cell	Non-selected cell
Objective	Write error	Read disturbance Write error	Write disturbance	Write disturbance
Organization	2WLs×2BLs	3WLs×3BLs	3WLs×5BLs 5WLs×3BLs	5WLs×5BLs

4.2.2 Simplified circuit for selected cell

The conventional simplified circuit introduced in Section 4.1 has the constraint that deviations in wire resistance according to the selected address are not taken into account. An example of this deviation is illustrated in Fig. 4.4. In addition, the conventional simplified circuit is not applicable to the analysis of read disturbances, which tend to occur in cells with low I_{TH}, as described in Fig. 2.10. Therefore, there is a difficulty in precisely calculating the BERs of read disturbances and write errors.

To overcome these constraints, a new simplified circuit that considers the wire resistance deviation and read disturbance is proposed. Figure 4.5 shows the new simplified circuit, which is composed of three WLs, three BLs, and nine memory elements. As illustrated in Fig. 4.6 [23][24], the center cell is defined as the (arbitrarily) selected cell from the original circuit in Fig. 2.3. The selected address is denoted as (k_R, k_C) in Fig. 4.5 for $1 \leq k_R \leq m$ and $1 \leq k_C \leq n$ [23][24]. The concept of this simplification is the same as that of the conventional simplified circuit.

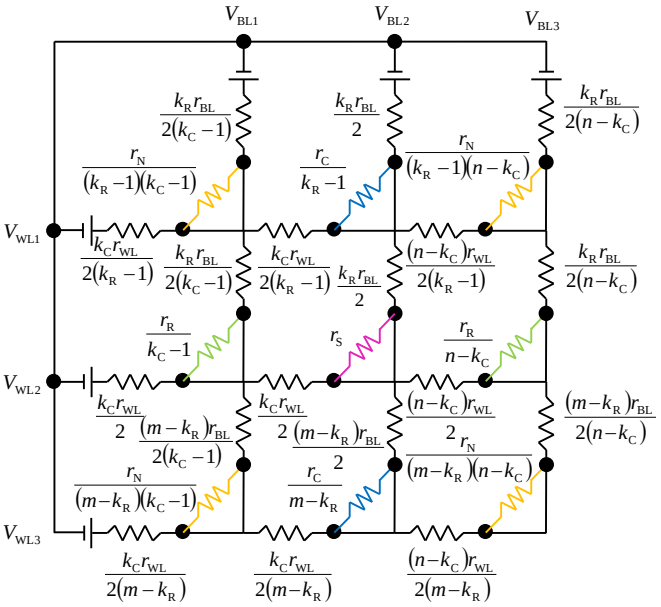
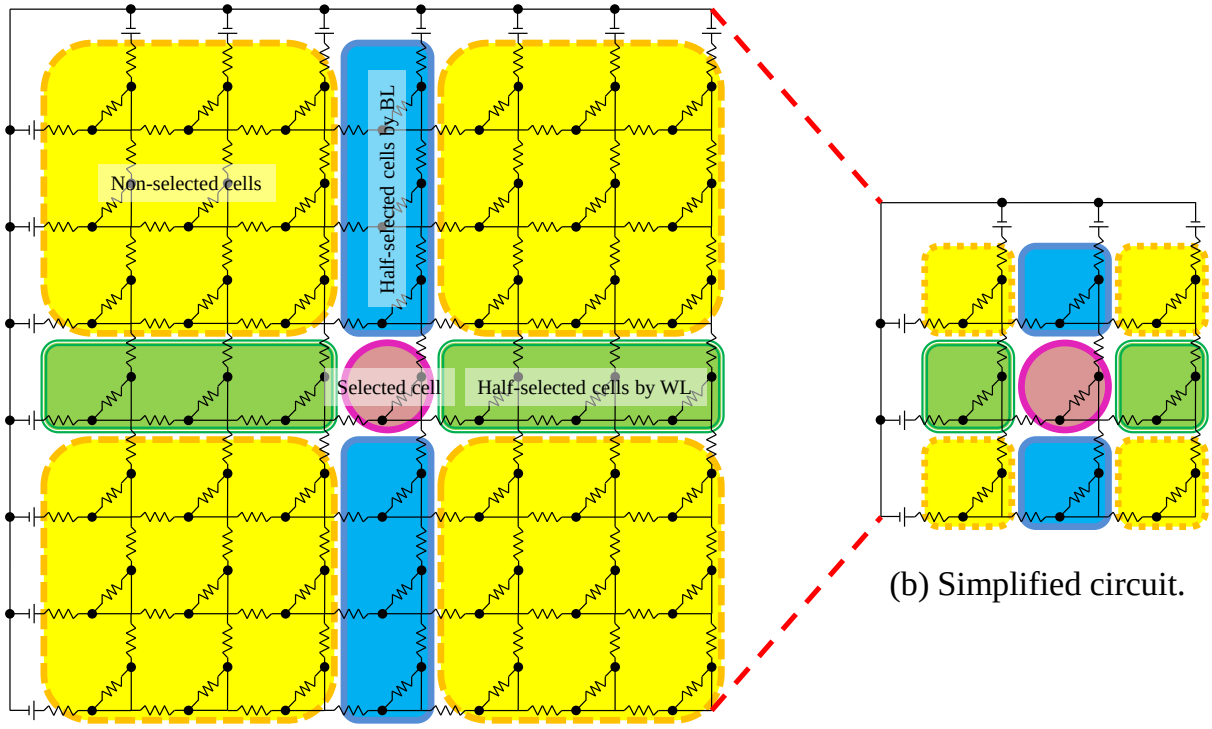


Fig. 4.5 Proposed simplified circuit for selected cell.



(b) Simplified circuit.

(a) Original circuit.

Fig. 4.6 Relationship between the original and the proposed simplified circuits.

4.2.3 Limitation of simplified circuit for selected cell

As described in Section 2.6, write disturbances cannot occur in unipolar writing memory, but can occur in bipolar writing memory. This is because there is a difference in the bias scheme between these two memories. During the SET[21] operation in bipolar writing memory, V_{DD}, 0V, $V_{DD}/2$, and $V_{DD}/2$ are applied to the selected WL, selected BL, non-selected WLs, and non-selected BLs, respectively. Conversely, during the RESET[22] operation, 0V, V_{DD}, $V_{DD}/2$, and $V_{DD}/2$ are applied to the selected WL, selected BL, non-selected WLs, and non-selected BLs, respectively. This is the $V_{DD}/2$ bias scheme for bipolar writing memory, which was briefly introduced in Fig. 2.7. If the wire resistance is neglected, $\pm V_{DD}/2$ is applied to the half-selected cells in which write disturbances can occur.

The $V_{DD}/3$ bias scheme can be discussed in a similar manner. As shown in Fig. 2.8, during the SET operation, V_{DD}, 0V, $V_{DD}/3$, and $2V_{DD}/3$ are applied to the selected WL, selected BL, non-selected WLs, and non-selected BLs, respectively. Conversely, for the RESET operation, 0V, V_{DD}, $2V_{DD}/3$, and $V_{DD}/3$ are applied to the selected WL, selected BL, non-selected WLs, and non-selected BLs, respectively. If the wire resistance is neglected, $\pm V_{DD}/3$ is applied to the half-selected and non-selected cells in which write disturbances can occur.

However, the proposed simplified circuit for the selected cell in Fig. 4.5 is not applicable to write disturbances in bipolar writing memory, because there is no means for approximating the currents in the half-selected and non-selected cells. Thus, a monitored cell is required to approximate the current in the simplified circuit. In Subsections 4.2.4 and 4.2.5, new simplified circuits are proposed. These overcome the limitation of the simplified circuit for the selected cell by adding a monitored cell.

4.2.4 Simplified circuit for half-selected cells

The proposed simplified circuit for the selected cell discussed in Subsections 4.2.2 and 4.2.3 has the constraint that the half-selected and non-selected cell currents cannot be calculated. Thus, the circuit is not applicable to the estimation of write disturbances. To overcome this constraint, two new simplified circuits are proposed for calculating the half-selected and non-selected cell currents. This subsection describes a new simplified circuit for calculating the half-selected cell currents.

Let us define (k_R, h_C) and (h_R, k_C) as the half-selected cell addresses corresponding to a WL and a BL, respectively. There are four positional relationships between the half-selected and selected cells, as illustrated in Fig. 4.7 [24], namely $h_C < k_C$, $h_C > k_C$, $h_R < k_R$, and $h_R > k_R$. In the first and second cases, the cells are selected by the WL to the left and right of the selected cell (k_R, k_C), respectively. In the third and fourth cases, the cells are selected by the BL above and below the selected cell, respectively. Figure 4.8 shows one of the proposed simplified circuits for the half-selected cell corresponding to the first case [24]. A monitored cell (2, 2) (shown in red) is prepared to approximate the WL half-selected cell current. The selected cell address is (2, 4). The relationship between the original and the proposed simplified circuit for the half-selected cell by the WL is shown in Fig. 4.9 [24]. The other three cases can be composed in a similar manner. Figures 4.10, 4.11, and 4.12 show the second, third, and fourth cases, respectively [24].

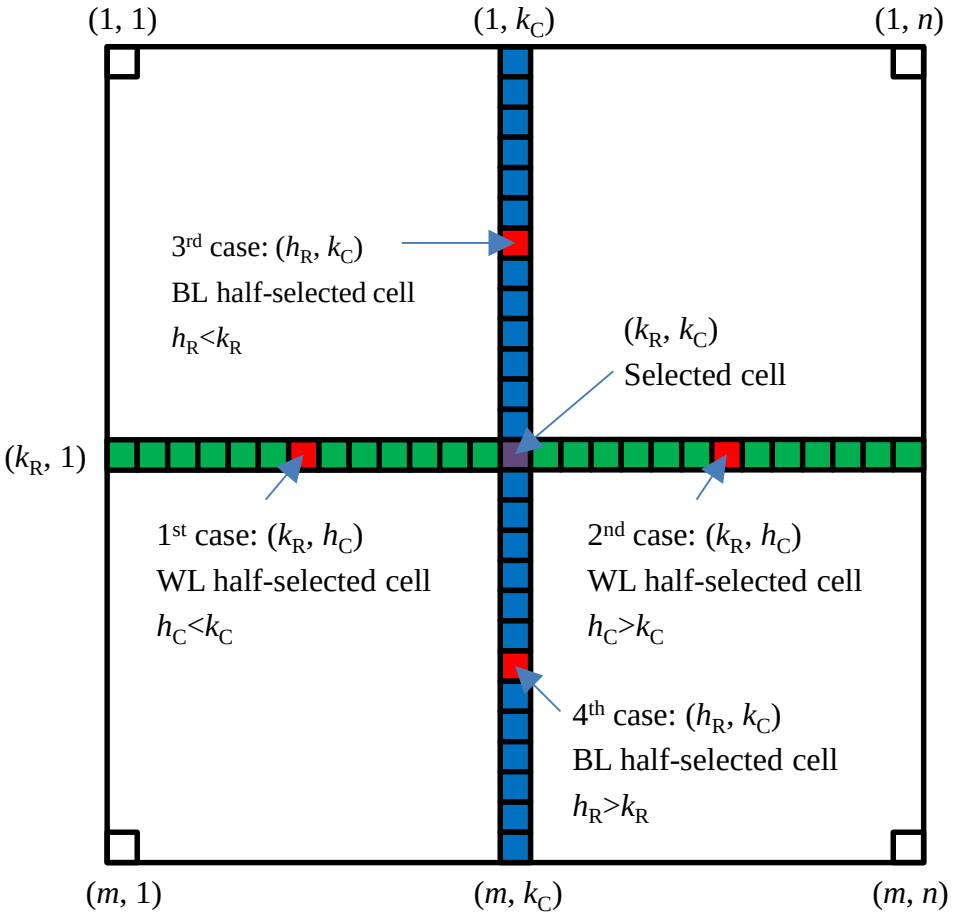


Fig. 4.7 Positional relationships between the half-selected and selected cells.

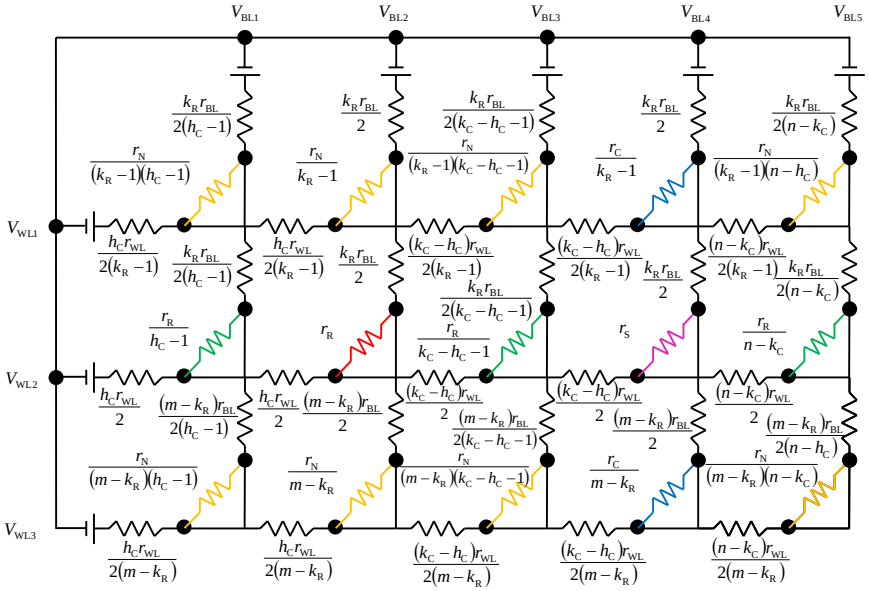
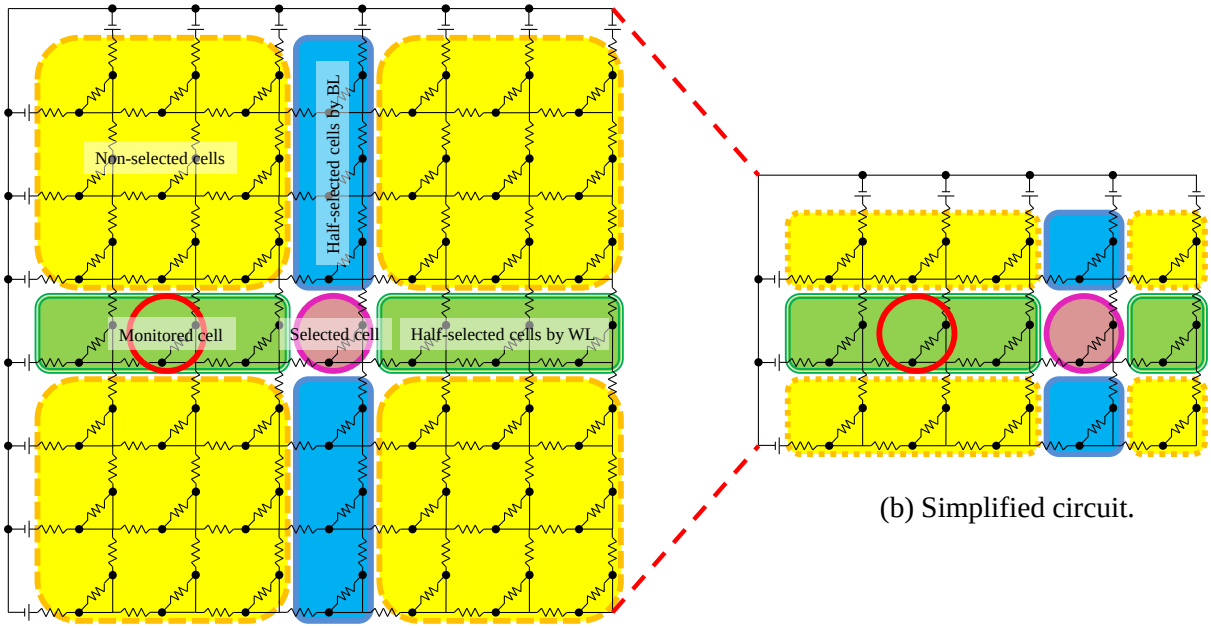


Fig. 4.8 Proposed simplified circuit for the half-selected cell in the first case.



(a) Original circuit.

(b) Simplified circuit.

Fig. 4.9 Relationship between the original and the proposed simplified circuits in the first case.

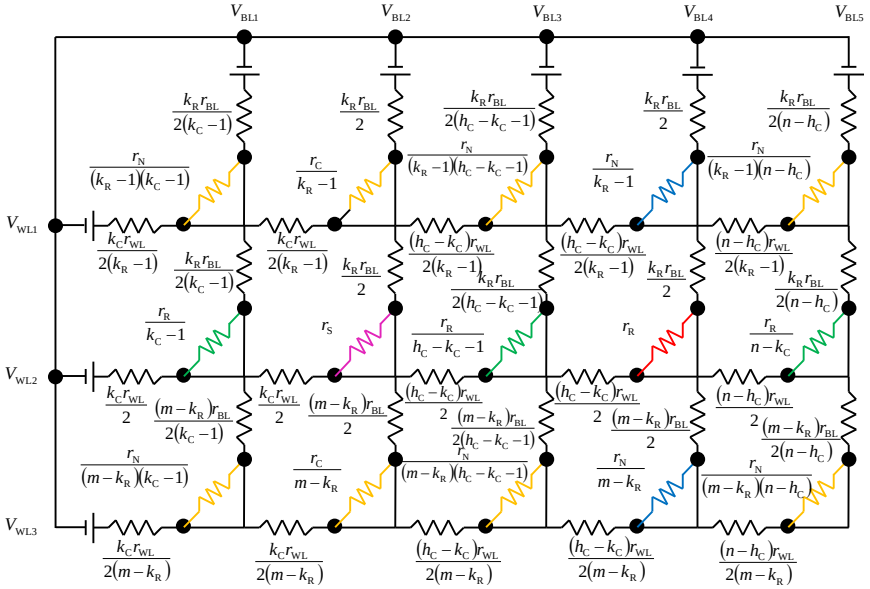


Fig. 4.10 Proposed simplified circuit for the half-selected cell in the second case.

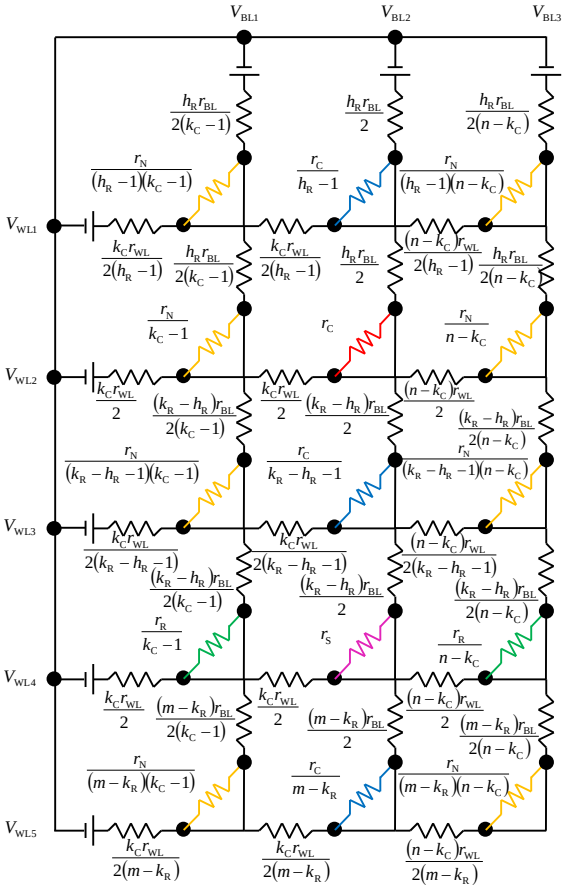


Fig. 4.11 Proposed simplified circuit for the half-selected cell in the third case.

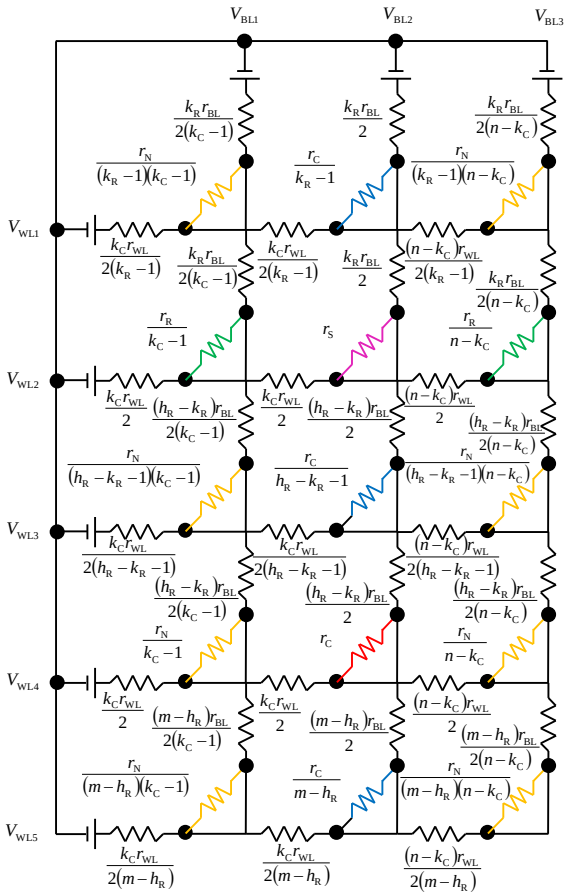


Fig. 4.12 Proposed simplified circuit for the half-selected cell in the fourth case.

4.2.5 Simplified circuit for non-selected cells

Write disturbances can occur in non-selected cells if the $V_{DD}/3$ bias scheme is used for bipolar writing memory, as discussed in Section 2.6. A simplified circuit for the non-selected cells is proposed below.

Let us define (h_R, h_C) to be a non-selected cell address. There are four positional relationships between the non-selected and selected cells, as illustrated in Fig. 4.13. In the first case, the non-selected cell is located to the upper left of the selected cell, namely $h_R < k_R$ and $h_C < k_C$. In the second case, the non-selected cell is located to the upper right of the selected cell, namely $h_R < k_R$ and $h_C > k_C$. In the third case, the non-selected cell is located to the lower left of the selected cell, namely $h_R > k_R$ and $h_C < k_C$. In the fourth case, the non-selected cell is

located to the lower right of the selected cell, namely $h_R > k_R$ and $h_C > k_C$. Figure 4.14 shows one of the proposed simplified circuits for non-selected cells corresponding to the first case [24]. A monitored cell (2, 2) (shown in red) is prepared to approximate the WL half-selected cell current. The selected cell address is (4, 4). The relationship between the original and proposed simplified circuits for non-selected cells is shown in Fig. 4.15 [24]. The other three cases can be composed in a similar manner. Figures 4.16, 4.17, and 4.18 show the second case, third case, and fourth case, respectively [24].

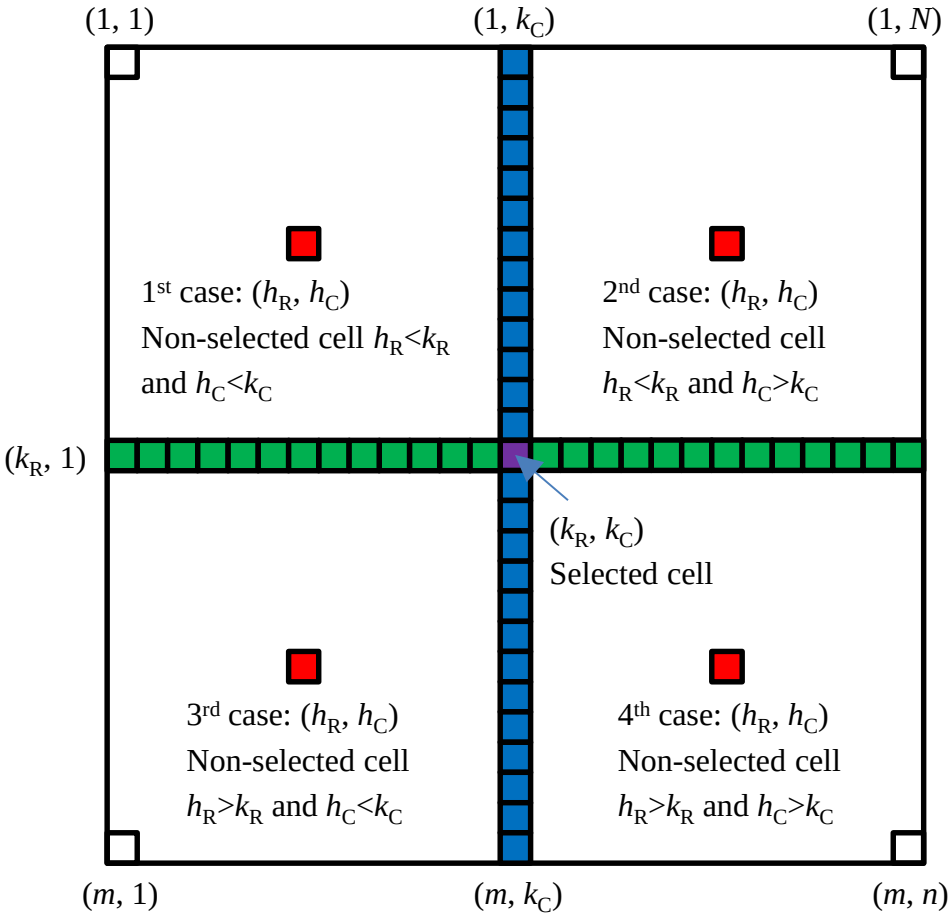


Fig. 4.13 Positional relationships between the non-selected and selected cells.

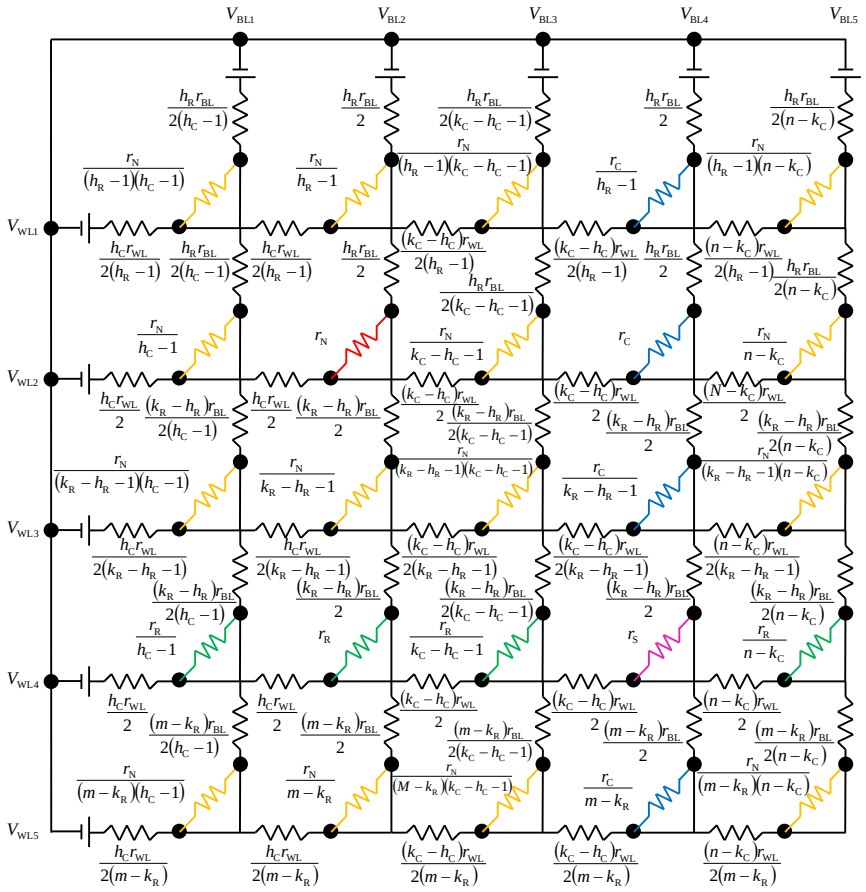
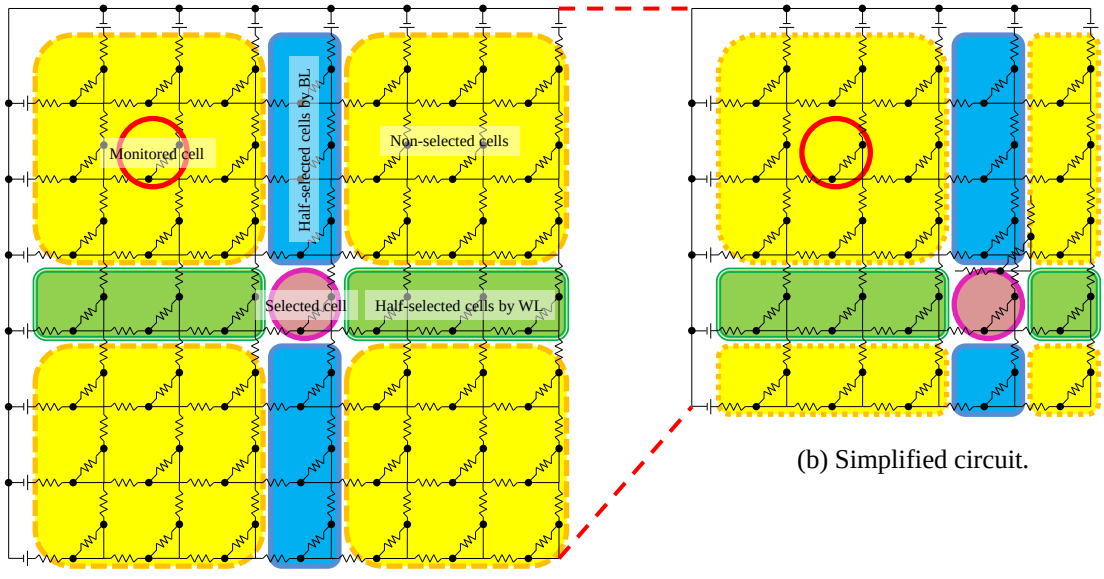


Fig. 4.14 Proposed simplified circuit for the non-selected cell in the first case.



(a) Original circuit.

(b) Simplified circuit.

Fig. 4.15 Relationship between the original and the proposed simplified circuits in the first case.

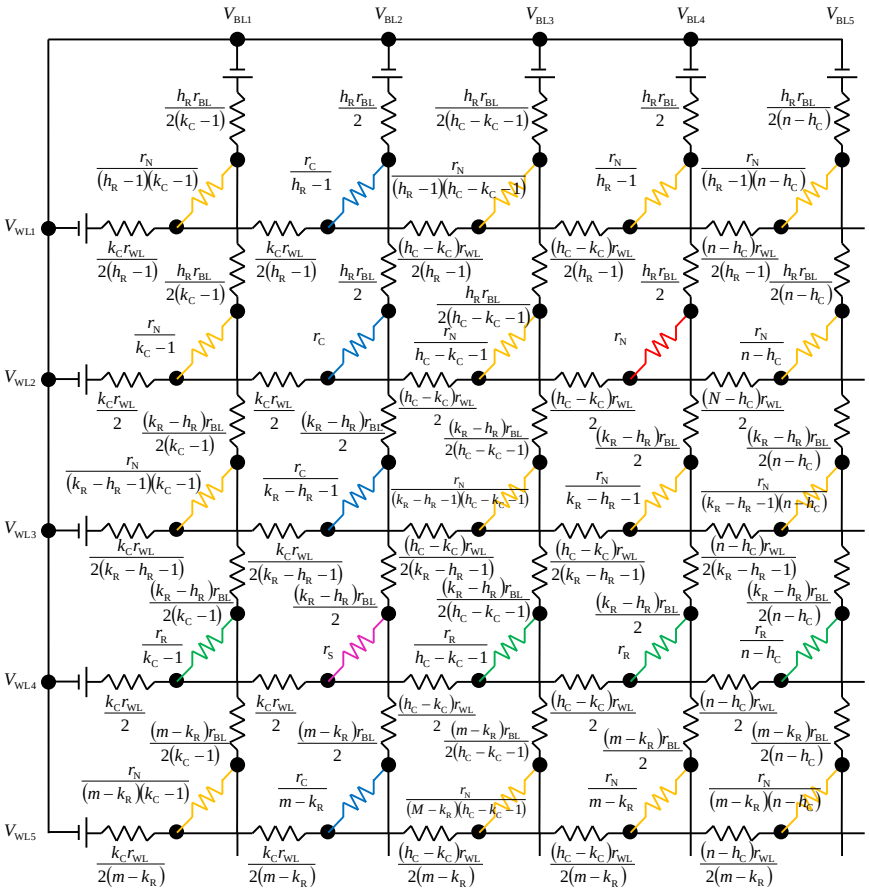


Fig. 4.16 Proposed simplified circuit for the non-selected cell in the second case.

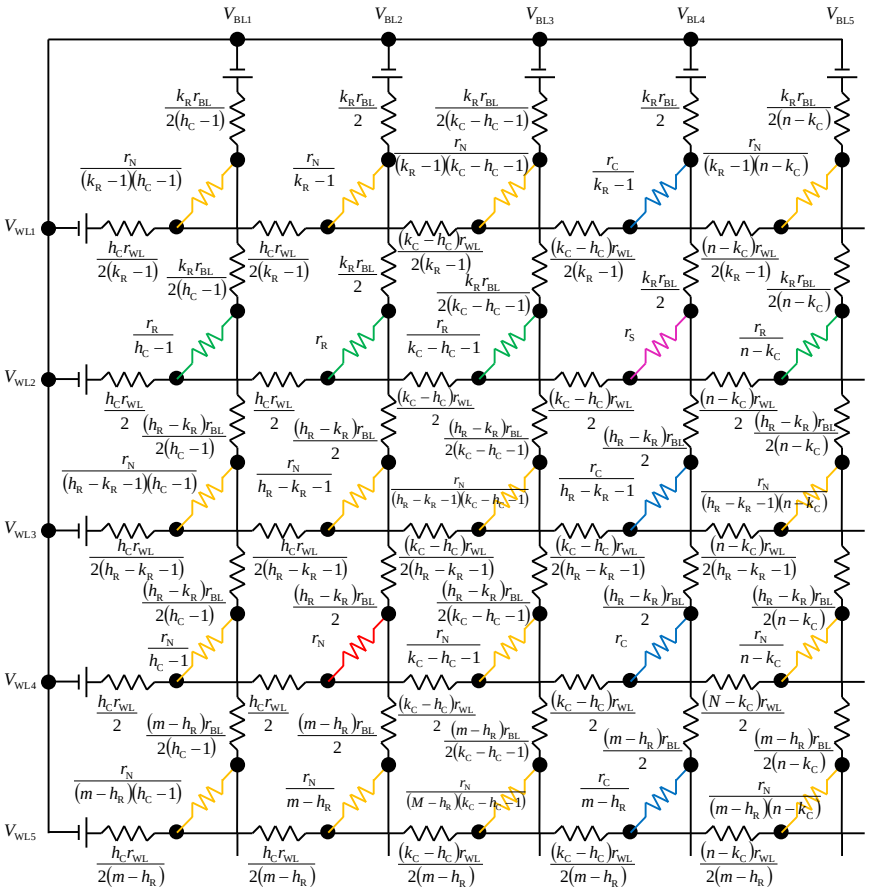


Fig. 4.17 Proposed simplified circuit for the non-selected cell in the third case.

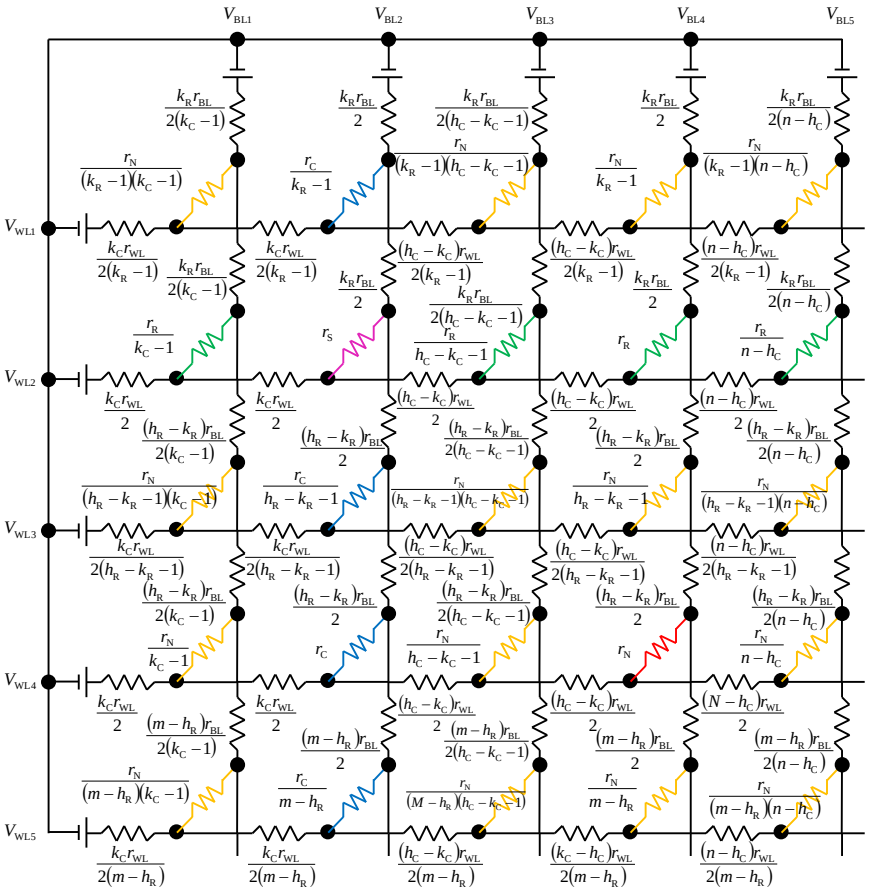


Fig. 4.18 Proposed simplified circuit for the non-selected cell in the fourth case.

4.3 Summary

The conventional simplified circuit has been widely used for calculating the cell current in the worst case. The calculated address is assumed to be located at the array corner, where the metal wire length is greatest. As a result, the calculated cell current is reduced by the wire resistance, giving the worst case for the write operation. However, read disturbances can occur when the read current is greater than the switching threshold current. The conventional simplified circuit cannot estimate this large read current, which may flow across any address in the cross-point array. Moreover, write disturbances can occur at the non-selected and half-selected addresses when a datum is written into the selected address. The conventional simplified circuit cannot estimate this disturbance current, which may flow across any address

in the cross-point array. To solve this problem, advanced simplified circuits for estimating the read disturbance current and the write disturbance current are proposed for fast computation with cross-point arrays.

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Chapter 5 Verification of the proposed simplified circuits

5.1 Parameters for verification

In Chapter 4, several simplified circuits were proposed for fast computation of the selected, half-selected, and non-selected cell currents. In this chapter, these circuits are verified by comparing the calculated current with that from the original circuit.

The verification parameters for unipolar writing memory are summarized in Table 5.1. The WL resistance r_{WL} of 4 Ω and the BL resistance r_{BL} of 4 Ω were derived from the MPU[25] wiring with a half-pitch of 18 nm, according to ITRS 2013 [32]. As illustrated in Fig. 2.9 (a), the memory element of unipolar writing memory has three resistance values, namely r_N in the non-selected state, $r_R = r_C$ in the half-selected state, and r_S in the selected state. It is assumed that the memory element includes the diode that limits the sneak current in the half-selected and non-selected states. Therefore, the half-selected cell resistance $r_R = r_C$ and the non-selected resistance r_N were set to 200 and 100 MΩ, respectively. The selected cell resistance r_S was set to 100 KΩ to simulate a low-resistance cell. In the selected state, the *I*−*V* curve has a hysteresis loop, where the memory element can be in either a high-resistance state (HRS)[26] or low-resistance state (LRS)[27]. Users can read data by sensing these two resistance states.

The verification parameters for bipolar writing memory are summarized in Table 5.2. Figure 2.9 (b) shows the *I*-*V* curve of bipolar writing memory. As described in Figs. 2.6, 2.7, and 2.8, there is a difference in the bias scheme between unipolar and bipolar writing memories. Therefore, the horizontal positions of the half-selection and non-selection of bipolar writing memory in Fig. 2.9 (b) are different from those of the unipolar one in Fig. 2.9 (a). The selected cell resistances r_S are 1 GΩ in HRS and 100 MΩ in LRS. These are designed to have little or no impact on the active power. In this case, the selected cell resistance r_S and the half-selected resistance $r_R = r_C$ share the same value, because the *I*−*V* curve is linear, as in Fig. 2.9 (b). The

$V_{DD}/2$ bias scheme has a non-selected resistance r_N of 100 GΩ because it is designed to suppress the sneak currents degrading the read and write margins. In the $V_{DD}/3$ scheme, the non-selected cells are biased by $\pm V_{DD}/3$ if the wire resistance is ignored. Thus, the non-selected cell resistance r_N is equal to the selected resistance r_S and the half-selected resistance r_H. During the SET operation in the $V_{DD}/3$ scheme, the non-selected cell is designed to be undisturbed under HRS but disturbed under LRS. In the same manner, during the RESET operation, the non-selected cell is designed to be undisturbed under LRS but disturbed under HRS.

Table 5.1 Calculation parameters for verification of the simplified circuit with unipolar writing memory [23].

Parameter	Symbol	Value
Selected cell resistance	r_S	100 KΩ
WL half-selected cell resistance	r_R	200 MΩ
BL half-selected cell resistance	r_C	200 MΩ
Non-selected cell resistance	r_N	100 MΩ
WL resistance	r_{WL}	4 Ω
BL resistance	r_{BL}	4 Ω
Selected WL voltage	V_{WL}	1 V
Non-selected WL voltage	V_{WL}	0 V
Selected BL voltage	V_{BL}	0 V
Non-selected BL voltage	V_{BL}	1 V

Table 5.2 Calculation parameters for verification of the simplified circuit with bipolar writing memory [24].

Parameter	Symbol	Value in HRS	Value in LRS
Selected cell resistance	r_S	1 GΩ	100 MΩ
WL half-selected cell resistance	r_R	1 GΩ	100 MΩ
BL half-selected cell resistance	r_C	1 GΩ	100 MΩ
Non-selected cell resistance in $V_{DD}/2$ bias scheme	r_N	100 GΩ	100 GΩ
Non-selected cell resistance in $V_{DD}/3$ bias scheme	r_N	1 GΩ	100 MΩ
WL resistance	r_{WL}	4 Ω	4 Ω
BL resistance	r_{BL}	4 Ω	4 Ω
Selected WL voltage	V_{WL}	V_{DD}	1 V
Non-selected WL voltage in $V_{DD}/2$ bias scheme	V_{WL}	$V_{DD}/2$	1/2 V
Non-selected WL voltage in $V_{DD}/3$ bias scheme	V_{WL}	$V_{DD}/3$	1/3 V
Selected BL voltage	V_{BL}	0 V	0 V
Non-selected BL voltage in $V_{DD}/2$ bias scheme	V_{BL}	$V_{DD}/2$	1/2 V
Non-selected BL voltage in $V_{DD}/3$ bias scheme	V_{BL}	$2V_{DD}/3$	2/3 V

5.2 Verification of the proposed simplified circuit and calculation time

Equation 2.4 was solved to calculate the selected cell current using the original circuit in Fig. 2.3 and the proposed simplified circuit for the selected cell in Fig. 4.5. The correlation between the calculated cell currents in these two circuits is plotted in Fig. 5.1. As a large mat size was applied (512×512), 50 addresses were randomly sampled to reduce the calculation time. Using the least-squares method, the line of best fit was obtained as $y = 1.00043x - 4.23595\times10^{-9}$ with a correlation coefficient of 1.0000. Thus, Fig. 5.1 indicates good agreement between these two circuits.

Note that the calculation time of the cell current shown in Fig. 5.1 was reduced by using the proposed simplified circuits. The calculation time with the original circuit was 18,369 s for 50 bits, whereas that with the proposed simplified circuits was 1 s for 50 bits. As indicated in Section 2.5, the calculation time depends on the mat size of the cross-point array. The simplified circuit has a mat size of 3×3. This result confirms that the proposed simplified circuit reduces the calculation time significantly compared to the original circuit.

The other two proposed circuits can be verified in the same manner as the above. Correlation plots of the calculated cell currents are shown in Figs. 5.2 and 5.3 for the half-selected cell and non-selected cell, respectively. Again, a large mat size was applied (512×512), and 50 addresses were randomly sampled to reduce the calculation time. The line of best fit in Fig. 5.2 is $y = 0.999985x + 7.73302\times10^{-15}$ with a correlation coefficient of 1.00000, demonstrating the good agreement between the original and simplified circuits. Figure 5.3 has a best fit line of $y = 0.999945x + 1.86300\times10^{-13}$ with a correlation coefficient of 1.00000, again demonstrating the good fit between the original and simplified circuits. (The simplified circuits for the half-selected cell are shown in Figs. 4.8, 4.10, 4.11, and 4.12; the simplified circuits for the non-selected cell are shown in Figs 4.14, 4.16, 4.17, and 4.18.)

The calculation time of the cell currents in Figs 5.2 and 5.3 was reduced by using the proposed simplified circuits. As mentioned in Section 2.5, the program was coded in C and was executed by a computer with 4 GB DRAM and a 3.4 GHz processor. The calculation time for the original circuit in Figs 5.2 and 5.3 was 21,047 s for 50 bits, whereas that for the proposed simplified circuits was 1 s for 50 bits. This confirms that the proposed simplified circuits can reduce the calculation time compared to the original circuits.

In conclusion, the three simplified circuits proposed in Chapter 4 have been successfully verified by comparing the calculated cell currents with those in the original circuits.

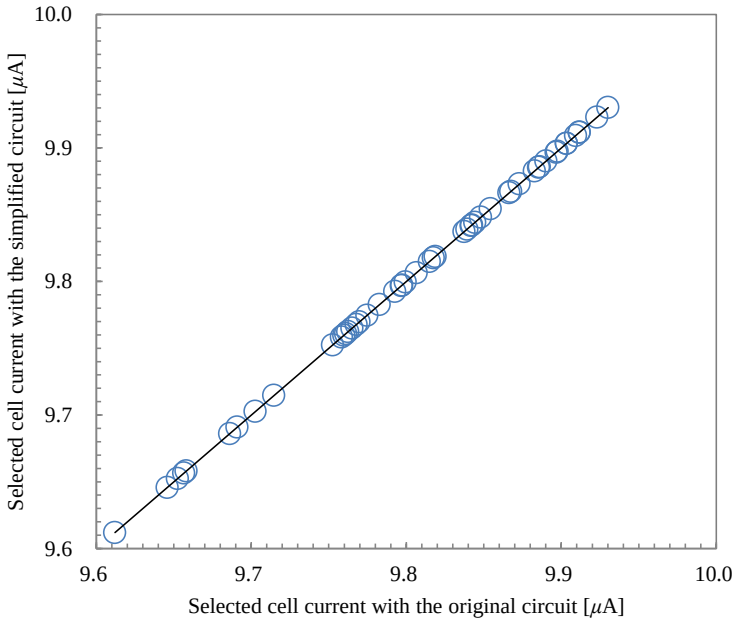


Fig. 5.1 Correlation of the selected cell current between the simplified and original circuits. The mat size is 512×512. Line of best fit is $y = 1.00043x - 4.23595\times10^{-9}$ with a correlation coefficient of 1.0000.

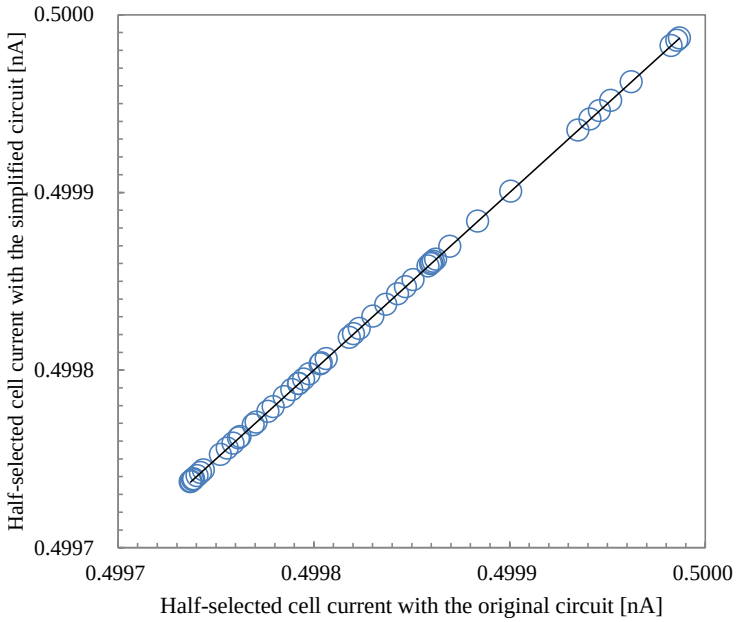


Fig. 5.2 Correlation of the half-selected cell current between the original and simplified circuits. The mat size is 512×512. Line of best fit is $y = 0.999985x + 7.73302\times10^{-15}$ with a correlation coefficient of 1.00000 [24].

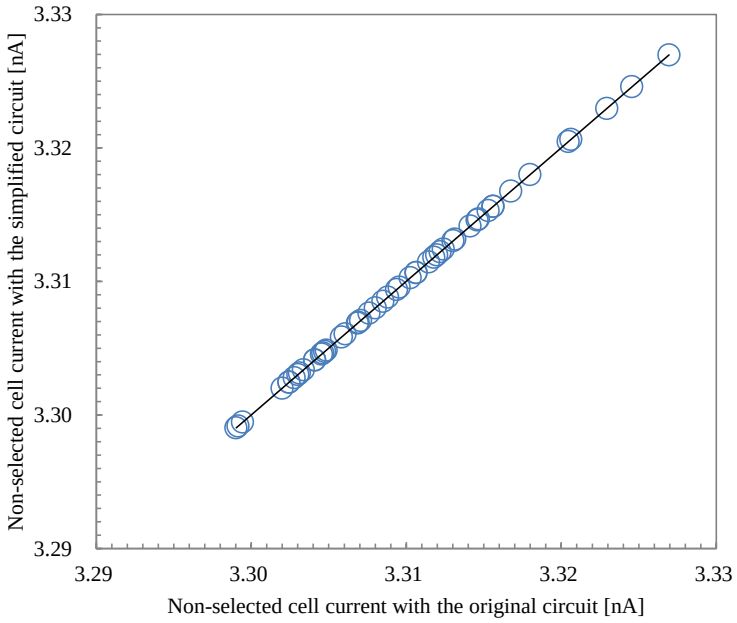


Fig. 5.3 Correlation of the non-selected cell current between the original and simplified circuits. The mat size is 512×512. Line of best fit is $y = 0.999945x + 1.86300\times10^{-13}$ with a correlation coefficient of 1.00000 [24].

5.3 Summary

The proposed simplified circuits were verified by comparing the calculated cell currents with those in the original circuits. The results indicate that the simplified circuits give an accurate representation of the cell currents. Using these simplified circuits, the critical issues faced by cross-point arrays can be discussed in Chapter 7.

References

[32]ITRS 2013 Edition (translated by JEITA), Table INTC11.

Chapter 6 Calculation sequence

6.1 Calculation sequence

In this section, a calculation sequence for estimating the BERs induced by disturbances and write errors is described using the techniques discussed in the previous chapters. The sequence is as follows [24]:

Step 1 Definition of device parameters.

Device parameters are determined. An example is presented in Table 6.1 for bipolar writing memory. The resistance of the resistive element, the applied voltage, number of wires, and threshold current are defined in Table 6.1.

Step 2 Random sampling of the monitored addresses for a Monte Carlo method[28].

The selected address (k_R, k_C), the WL half-selected address (k_R, h_C), the BL half-selected address (h_R, k_C), and the non-selected address (h_R, h_C) are randomly sampled.

Step 3 Definition of statistical parameters for the resistance.

Random numbers obeying the normal distribution are generated for the resistance of the resistive elements and the threshold currents. The expectation and standard deviation of the connected resistance are summarized in Table 2.1. Note that some of the resistive elements are approximated in the simplified circuits using series or parallel connections. Therefore, statistical approximation is required to determine the standard deviation of such resistive elements. Details are described in Section 6.2.

Step 4 Cell current calculation.

The selected, half-selected, and non-selected cell currents are calculated by applying Kirchhoff's laws (Eq. 2.4) to the simplified circuits.

Step 5 Statistical estimation of the cell current using the Monte Carlo method.

By repeating Steps 2–4, the expectation μ and standard deviation σ of the cell current are estimated for the selected, half-selected, and non-selected cell currents. In this study, this step was repeated 1000 times to obtain statistically accurate values of μ and σ. As described in Section 7.1.1, the calculated cell current is distributed according to the log-normal distribution, with a significance level of 5% used as the criterion for random sampling.

Step 6 Calculation of the BERs caused by disturbances and write errors.

The BERs caused by the disturbances and write errors are consequently obtained using Eqs. 3.2 and 3.3, respectively.

The calculation time for 1000 loops of Steps 1–5 was 6.46 s. In addition, it took 1.11 s for Step 6 to obtain each BER. Note that the proposed sequence is sufficiently fast that it would be a comprehensive tool for the design of large-scale memory.

Table 6.1 Calculation parameters for bipolar writing memory [24].

Parameter	Symbol	Value
Selected cell resistance in HRS	r_S	1×10^9 Ω
Selected cell resistance in LRS	r_S	1×10^8 Ω
WL half-selected cell resistance in HRS	r_R	1×10^9 Ω
WL half-selected cell resistance in LRS	r_R	1×10^8 Ω
BL half-selected cell resistance in HRS	r_C	1×10^9 Ω
BL half-selected cell resistance in LRS	r_C	1×10^8 Ω
Non-selected cell resistance (V_{DD}/2 bias scheme)	r_N	1×10^{11} Ω
Non-selected cell resistance in HRS (V_{DD}/3 bias scheme)	r_N	1×10^9 Ω
Non-selected cell resistance in LRS (V_{DD}/3 bias scheme)	r_N	1×10^8 Ω
WL resistance	r_{WL}	4 Ω
BL resistance	r_{BL}	4 Ω
Selected WL voltage	V_{WL}	V_{DD}
Non-selected WL voltage (V_{DD}/2 bias scheme)	V_{WL}	V_{DD}/2
Non-selected WL voltage (V_{DD}/3 bias scheme)	V_{WL}	V_{DD}/3
Selected BL voltage	V_{BL}	0 V
Non-selected BL voltage (V_{DD}/2 bias scheme)	V_{BL}	V_{DD}/2
Non-selected BL voltage (V_{DD}/3 bias scheme)	V_{BL}	$2V_{DD}$/3
Number of WLs	m	512
Number of BLs	n	512
Threshold current for SET	I_{TH}	2 nA
Threshold current for RESET	I_{TH}	20 nA

6.2 Standard deviation of series and parallel resistors

The simplified circuits have several series and parallel resistors. If a Monte Carlo method[28] is applied to the resistors, an approximation technique is required to obtain the associated standard deviations.

There are three types of resistor connections, as shown in Fig. 6.1. These are series, parallel, and series–parallel combination connections. Let us define μ and σ as the expectation and standard deviation of a resistor population, respectively. If m resistors are chosen from the population and connected in series, as in Fig. 6.1 (a), the series resistance y is given as

$$y = x_1 + x_2 + \cdots + x_m, \qquad \text{Eq. 6.1}$$

where x_i is the resistance of a resistor for i = 1, 2, ⋯, m. From the central limit theorem [33],

the expectation μ_{series} and the standard deviation σ_{series} of the series resistance y are given by

$$\mu_{\text{series}} = m\mu, \quad \text{Eq. 6.2}$$

$$\sigma_{\text{series}} = \sqrt{m}\sigma, \quad \text{Eq. 6.3}$$

respectively.

When n resistors are chosen from the population and connected in parallel, as illustrated in Fig. 6.1 (b), the parallel resistance z is given by

$$z = \frac{1}{\frac{1}{x_1} + \frac{1}{x_2} + \cdots + \frac{1}{x_n}}, \quad \text{Eq. 6.4}$$

where x_i is the resistance of a resistor for $i = 1, 2, \cdots, n$. From the law of the propagation of error [34], the expectation μ_{parallel} and σ_{parallel} are approximated as

$$\mu_{\text{parallel}} = \frac{\mu}{n}, \quad \text{Eq. 6.5}$$

$$\sigma_{\text{parallel}} = \sqrt{\left(\frac{\partial z}{\partial x_1}\right)^2 \sigma_{x_1}^2 + \left(\frac{\partial z}{\partial x_2}\right)^2 \sigma_{x_2}^2 + \cdots + \left(\frac{\partial z}{\partial x_n}\right)^2 \sigma_{x_n}^2}, \quad \text{Eq. 6.6}$$

respectively. Let us define σx_i as the standard deviation of x_i for $i = 1, 2, \cdots, n$. By partially differentiating z with respect to x_i in Eq. 6.4, it is found that

$$\frac{\partial z}{\partial x_i} = \frac{\frac{1}{x_i^2}}{\left(\frac{1}{x_1} + \frac{1}{x_2} + \cdots + \frac{1}{x_n}\right)^2}, \quad \text{Eq. 6.7}$$

for $i = 1, 2, \cdots, n$. As every resistor shares the same expectation μ, Eq. 6.7 becomes

$$\frac{\partial z}{\partial x_i} = \frac{\frac{1}{\mu^2}}{\left(\frac{n}{\mu}\right)^2} = \frac{1}{n^2}, \quad \text{Eq. 6.8}$$

for $i = 1, 2, \cdots, n$ [23]. Furthermore, as every resistor shares the same standard deviation σ, Eq. 6.6 can be written in the form [23]

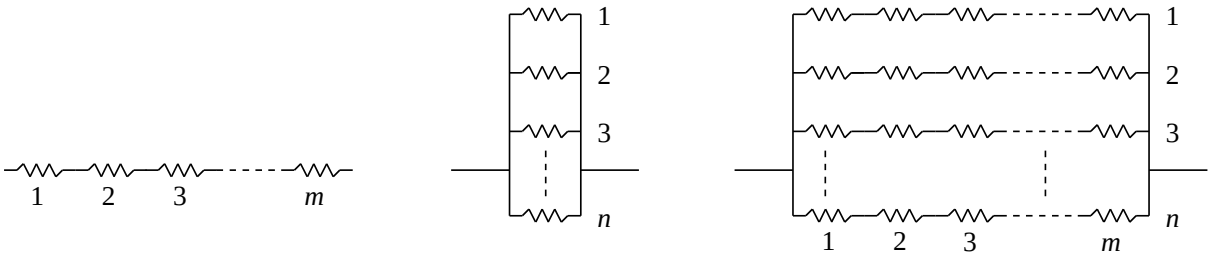
$$\sigma_{\text{parallel}} = \frac{\sigma}{n^{1.5}}. \qquad \text{Eq. 6.9}$$

If $m\times n$ resistors are connected in series and in parallel, as illustrated in Fig. 6.1 (c), the expectation $\mu_{\text{series-parallel}}$ and the standard deviation $\sigma_{\text{series-parallel}}$ of the series–parallel resistance are given by

$$\mu_{\text{series-parallel}} = \frac{m}{n}\mu, \qquad \text{Eq. 6.10}$$

$$\sigma_{\text{series-parallel}} = \frac{\sqrt{m}}{n^{1.5}}\sigma, \qquad \text{Eq. 6.11}$$

respectively [23]. Table 6.2 summarizes the connected resistors discussed here. Using Table 6.2, random numbers can be generated to calculate the cell current in the simplified circuits.



(a) Series. (b) Parallel. (c) Series-parallel.

Fig. 6.1 Types of resistor connections [23].

Table 6.2 Expectation and standard deviation of connected resistors [23].

	Series	Parallel	Series–Parallel
Number of resistors	m	n	$m\times n$
Expectation	$m\mu$	$\frac{1}{n}\mu$	$\frac{m}{n}\mu,$
Standard deviation	$\sqrt{m}\sigma$	$\frac{1}{n^{1.5}}\sigma$	$\frac{\sqrt{m}}{n^{1.5}}\sigma,$

6.3 Summary

The calculation sequence for estimating the BERs induced by disturbances and write errors has been described. The sequence is composed of six steps. The device parameters of the resistance of the resistive element, the applied voltage, number of wires, and threshold current are defined in Step 1. Then, the selected, WL half-selected, BL half-selected, and non-selected addresses are randomly sampled in Step 2. In Step 3, random numbers obeying the normal distribution are generated for the resistance of the resistive elements and the threshold currents. In Step 4, these parameters are used to calculate the selected, half-selected, and non-selected cell currents by applying Kirchhoff's laws to the simplified circuits. By repeating Steps 2–4, the statistical data of the cell current are estimated. Consequently, the BERs caused by disturbances and write errors are obtained.

The calculation time for 1000 loops of Steps 1–5 was 6.46 s. In addition, it took 1.11 s for Step 6 to obtain each BER. The proposed sequence is sufficiently fast that it represents a comprehensive tool for the design of large-scale memory.

References

[33] H. Cramér, ed., Mathematical Methods of Statistics, Princeton University Press, USA, 1946.

[34] H. H. Ku, "Notes on the use of propagation of error formulas," Journal of Research of National Bureau of Standards −C. Engineering and Instrumentation, vol. 70C, no. 4, pp. 263−273, 1996.

Chapter 7 Calculation results

7.1 Trade-off relationship between read disturbances and write errors in unipolar writing memory

7.1.1 Calculation of BERs induced by read disturbances and write errors with the simplified circuits

The trade-off relationship between read disturbances and write errors is estimated using the simplified circuit for the selected cell (Fig. 4.5). The calculation is carried out in accordance with the sequence described in Section 6.1.

For Step 1, the calculation parameters are summarized in Table 7.1. As summarized in Table 2.1, the read disturbances and write errors can be observed in both unipolar and bipolar writing memories. Here, unipolar writing memory is used for the BER estimation.

For Step 2, 1000 selected addresses (k_{Ri}, k_{Ci}) are randomly sampled for $1 \leq k_{Ri} \leq m$, $1 \leq k_{Ci} \leq n$, and $i = 1, 2, \cdots, 1000$.

For Step 3, the resistance values of the resistive elements are generated by a Monte Carlo simulation assuming a normal distribution. The standard deviations of the series and parallel resistors used in the simplified circuit are described in Section 6.2. For instance, part of the selected BL in Fig. 4.5 has resistance $k_R r_{BL}/2$, where $k_R/2$ BL elements are connected in series. If the standard deviation of r_{BL} is 5%, that of $k_R r_{BL}/2$ is $(k_R/2)^{1/2} \times 6\%$ from Eq. 6.3.

For Steps 4 and 5, 1000 selected cell currents are calculated by solving Eq. 2.4. The calculated cell currents obey a log-normal distribution according to the chi-squared test[29] [33]. The application of the chi-squared test for log-normal and normal distributions is described in Table 7.2, where the standard deviation of the resistive elements, V_{DD}, and the mat size are 6%, 1 V, and 4096×4096, respectively. Let O_i and E_i be the observed cell current frequency and the expected frequency from the theoretical distribution in the i-th class, respectively. The

parameter χ^2 is distributed in a chi-squared distribution with N degrees of freedom[30]:

$$\chi^2 = (O_1 - E_1)^2 + (O_2 - E_2)^2 + \cdots + (O_M - E_M)^2. \quad \text{Eq. 7.1}$$

N is defined as

$$N = M - 1 - t, \quad \text{Eq. 7.2}$$

where t is the number of estimated parameters. The log-normal and normal distributions have two estimated parameters, namely the expectation and standard deviation. If χ^2 is sufficiently small, the cell current obeys the theoretical distribution. In Table 7.2, N = 16 because M and t are 19 and 2, respectively. If the significant level[31] and N are 5% and 16, respectively, χ^2 = 26.296 [33]. This value of χ^2 is greater than the total $(O_i - E_i)^2/E_i$ = 17.65 for the log-normal distribution in Table 7.2 [23]. Thus, the cell current obeys the log-normal distribution. In contrast, χ^2 is less than the total of $(O_i - E_i)^2/E_i$ = 42.06 for the normal distribution. Consequently, the cell current does not obey the normal distribution.

If the cell current obeys the log-normal distribution, Eq. 3.1 can be transformed to

$$f(x,y) = \frac{1}{2\pi\sigma_x\sigma_y\sqrt{1-\rho^2}y}\,\mathrm{e}^{-\frac{1}{2(1-\rho^2)}\left[\frac{(x-\mu_x)^2}{\sigma_x^2} - \frac{2\rho(x-\mu_x)(\log y-\mu_z)}{\sigma_x\sigma_z} + \frac{(\log y-\mu_z)^2}{\sigma_z^2}\right]}, \quad \text{Eq. 7.3}$$

where μ_z and σ_z are given by

$$\mu_z = \log\left(\frac{\mu_y^2}{\sqrt{\mu_y^2+\sigma_y^2}}\right), \quad \text{Eq. 7.4}$$

$$\sigma_z = \sqrt{\log\left(\frac{\mu_y^2+\sigma_y^2}{\mu_y^2}\right)}, \quad \text{Eq. 7.5}$$

respectively [35].

Finally, for Step 6, the BERs caused by read disturbances and write errors can be obtained as a function of V_{DD} by solving Eqs. 3.2 and 3.3, respectively.

Table 7.1 Calculation parameters for estimating read disturbance and write error [23].

Parameter	Symbol	Expectation	Standard deviation
Selected cell resistance	r_S	100 KΩ	2−10%
WL half-selected cell resistance	r_R	100 TΩ	2−10%
BL half-selected cell resistance	r_C	100 TΩ	2−10%
Non-selected cell resistance	r_N	10 TΩ	2−10%
WL resistance	r_{WL}	4 Ω	2−10%
BL resistance	r_{BL}	4 Ω	2−10%
Selected WL voltage	V_{WL}	V_{DD}	
Non-selected WL voltage	V_{WL}	0 V	
Selected BL voltage	V_{BL}	0 V	
Non-selected BL voltage	V_{BL}	V_{DD}	
Number of WLs	m	1024 − 8192	
Number of BLs	n	1024 − 8192	
Threshold current	I_{TH}	10 μA	8%
Correlation efficient of I_{CELL} and I_{TH}	ρ	0	

Table 7.2 Application of the chi-squared test to the log-normal and normal distributions [23].

			Log-normal		Normal	
i	I_{CELL} [μA]	O_i	E_i	$(O_i\text{-}E_i)^2/E_i$	E_i	$(O_i\text{-}E_i)^2/E_i$
1	− 7.2	8	9.2	0.15	14.4	2.88
2	7.2 − 7.4	8	13.1	2.01	15.0	3.25
3	7.4 − 7.6	24	25.8	0.12	26.3	0.20
4	7.6 − 7.8	40	44.2	0.39	42.2	0.11
5	7.8 – 8.0	83	66.8	3.46	62.0	6.46
6	8.0 – 8.2	95	89.9	0.29	83.3	1.63
7	8.2 – 8.4	120	108.7	1.18	102.5	2.99
8	8.4 − 8.6	105	118.7	1.59	115.3	0.93
9	8.6 – 8.8	119	118.2	0.01	118.8	0.00
10	8.8 – 9.0	110	107.8	0.05	111.9	0.03
11	9.0 – 9.2	95	90.6	0.22	96.5	0.03
12	9.2 − 9.4	56	70.5	2.99	76.1	5.30
13	9.4 − 9.6	45	51.2	0.74	54.9	1.79
14	9.6 – 9.8	36	34.7	0.05	36.3	0.00
15	9.8 – 10.0	18	22.1	0.77	21.9	0.70
16	10.0 – 10.2	18	13.3	1.67	12.1	2.87
17	10.2 – 10.4	10	7.6	0.79	6.1	2.45
18	10.4 – 10.6	5	4.1	0.20	2.8	1.66
19	10.6 – 10.8	2	2.1		1.2	
20	10.8 – 11.0	3	1.0		0.5	
21	11.0 – 11.2	0	0.5	0.99	0.2	8.80
22	11.2 – 11.4	0	0.2		0.1	
23	11.4 –	1	0.2		0.0	
	Total	1000	1000.3	17.65	1000.3	42.06

7.1.2 Calculation results for the trade-off relationship between read disturbances and write errors

The differences between the conventional and proposed simplified circuits are now discussed by calculating the BER. Figures 7.1 and 7.2 show the BERs of the read disturbances calculated with the conventional simplified circuit (Fig. 4.1) and the proposed simplified circuit for the selected cell (Fig. 4.5), respectively. They are plotted as a function of read voltage V_{DD}. The read disturbance can be improved either by decreasing V_{DD} or decreasing the standard deviation of the resistive elements σ. In the same manner, Figs. 7.3 and 7.4 show the BERs of the write errors calculated with the conventional and proposed simplified circuits for the

selected cell, respectively. Conversely, the write error can be improved by increasing the write voltage V_{DD}.

Suppose that the read and the write voltages are 1 V and 3 V, respectively. The conventional simplified circuit gives lower values for the read disturbance and write error than the proposed circuit. That is, the conventional one gives optimistic results. To clarify this result, the mat size dependence on the BERs was investigated, as shown in Fig. 7.5, where V_{DD} is plotted so that the BER is equal to 1×10^{-10}. Larger mat sizes enhance the differences in V_{DD} between the two circuits for the read disturbances and write errors. This indicates that the wire length is related to the phenomena whereby the conventional simplified circuit gives optimistic results compared to the proposed one.

Figure 7.6 shows the expectation μ_y and standard deviation σ_y of the cell current as a parameter of the mat size. Larger mat sizes lead to a greater decrease in μ_y for the conventional simplified circuit than for the proposed one. This is because the wire length as a current path is constant in the conventional simplified circuit, as shown in Fig. 4.1, whereas the wire length as a current path varies with the selected address in the proposed simplified circuit, as shown in Fig. 4.5.

Therefore, the conventional simplified circuit has a larger average wire length than the proposed simplified circuit. The larger mat sizes lead to a decrease in σ_y for the conventional simplified circuit and an increase in σ_y for the proposed one. This is because the conventional simplified circuit has a smaller variation in wire length than the proposed circuit.

Examples of the frequency curves for the read current (I_{READ}), threshold current (I_{TH}), and write current (I_{WRITE}) are shown in Fig. 7.7, where the mat size is 8192×8192. The standard deviation of all resistive elements is 10%. The read and write voltages are 0.5 V and 3 V, respectively. It is assumed that I_{TH} obeys the normal distribution with an expectation of 10 μA

and standard deviation of 8%. Both the vertical and horizontal axes are logarithmic scales. The frequency curves of I_{READ} and I_{WRITE} using the conventional simplified circuit exhibit less overlap with I_{TH} than when using the proposed circuit. For the same V_{DD}, the conventional simplified circuit obviously gives lower values of the read disturbance and write error than the proposed circuit.

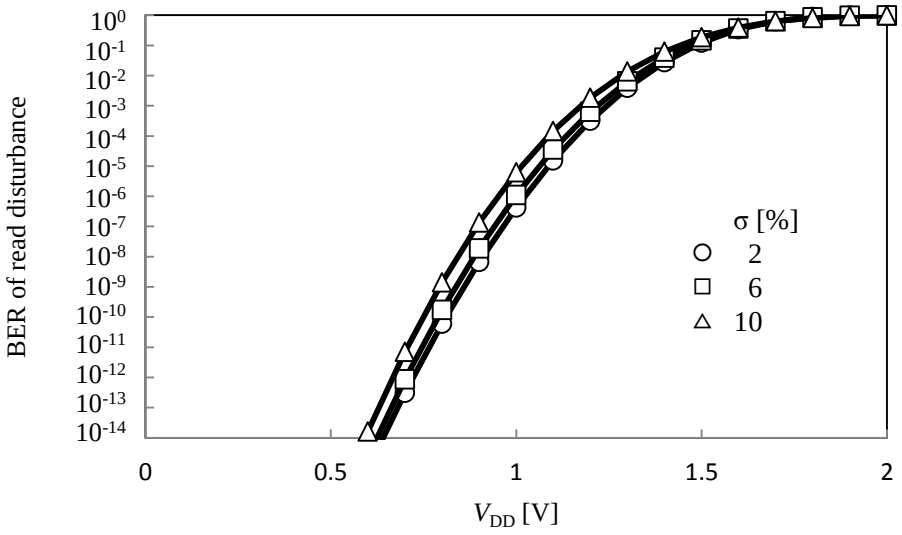


Fig. 7.1 BER of the read disturbance calculated with conventional simplified circuit [23].

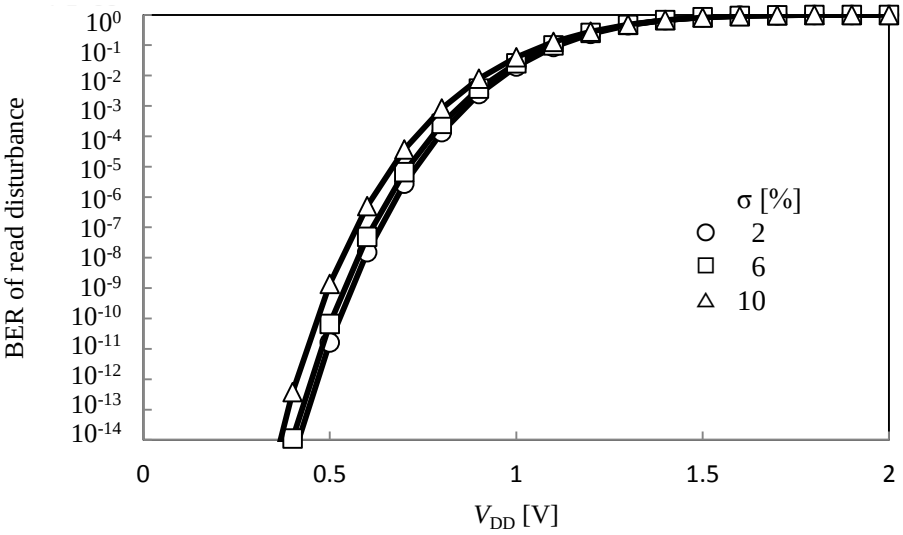


Fig. 7.2 BER of the read disturbance calculated with the proposed simplified circuit [23].

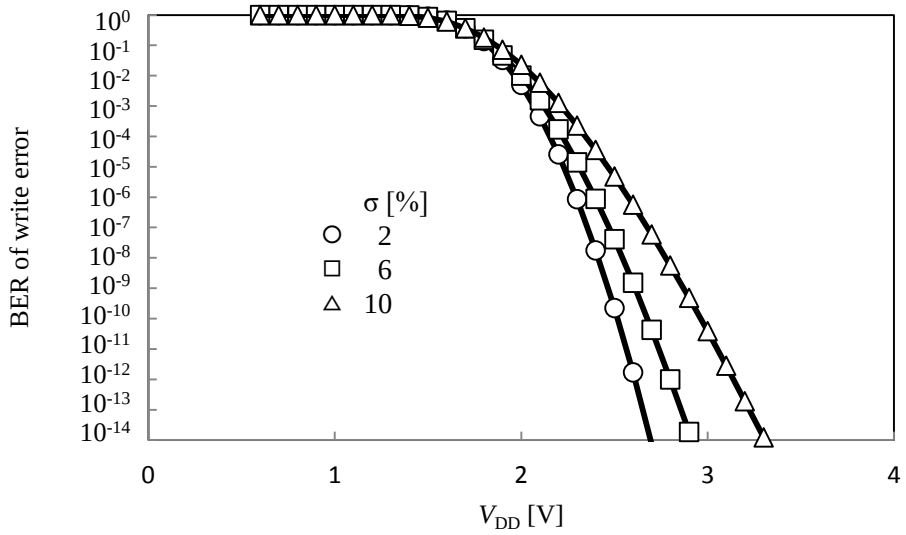


Fig. 7.3 BER of the write error calculated with the conventional simplified circuit [23].

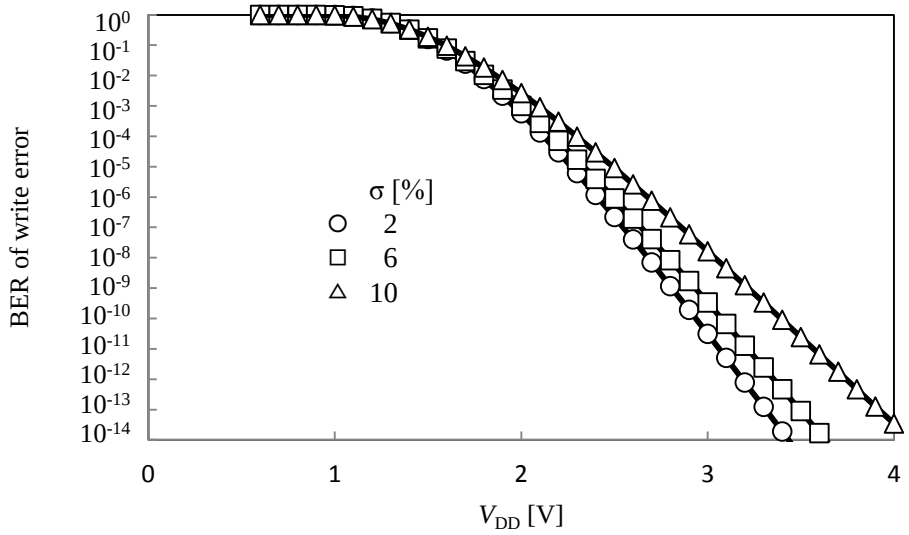


Fig. 7.4 BER of the write error calculated with the proposed simplified circuit [23].

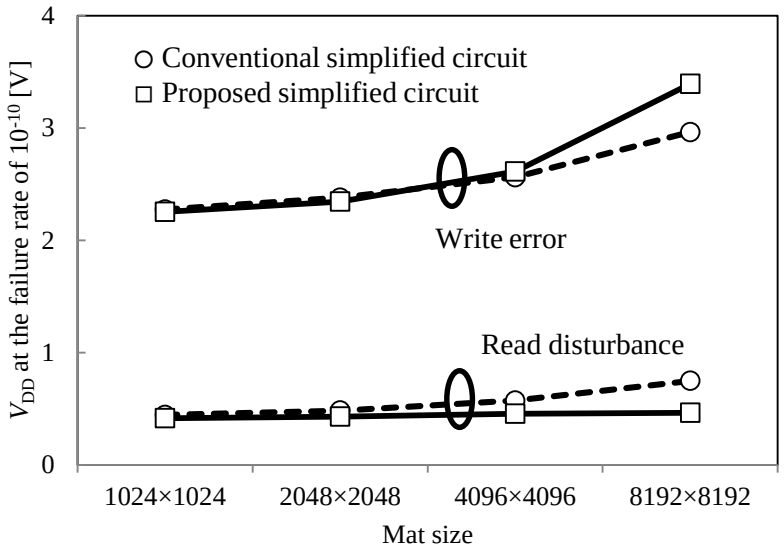


Fig. 7.5 Mat size dependence on the read disturbance and write error [23].

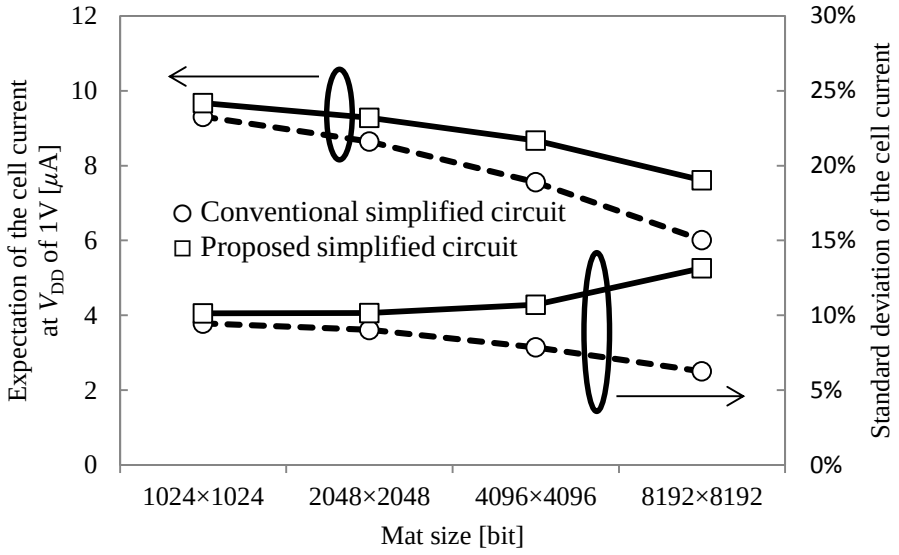


Fig. 7.6 Mat size dependence on the statistical parameters of the cell current [23].

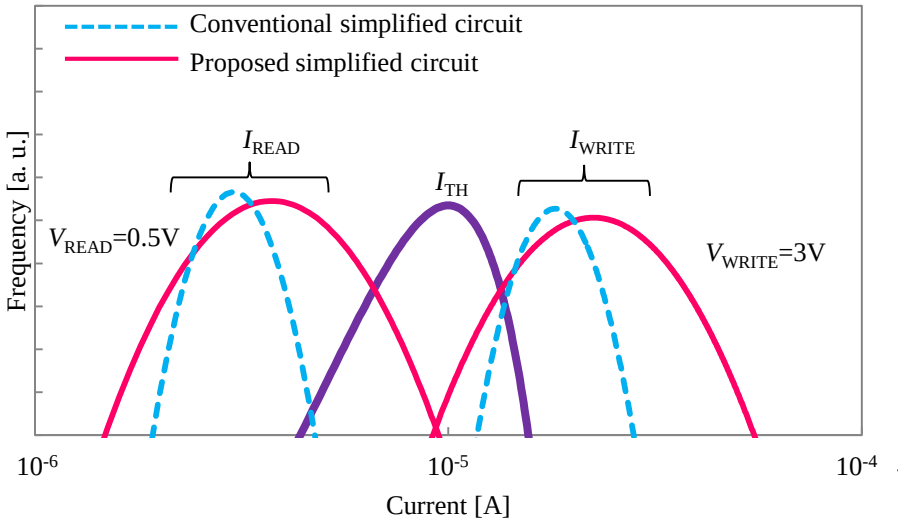


Fig. 7.7 Frequency curves of the read current (I_{READ}), threshold current (I_{TH}), and write current (I_{WRITE}) [23].

7.2 Trade-off relationship between write disturbances and write errors in bipolar writing memory

As discussed in Section 2.6, write disturbances can occur in bipolar writing memory. In this section, the trade-off relationship between write disturbances and write errors is estimated for bipolar writing memory.

Using the calculation sequence mentioned in Section 6.1, the BERs in the $V_{DD}/2$ and $V_{DD}/3$ bias schemes are calculated as a function of the write voltage V_{DD}, as shown in Figs. 7.8 and 7.9, respectively, for a mat size of 512×512. The calculation parameters are summarized in Table 7.3. The BER includes failures that occur during the SET and RESET operations. As high values of V_{DD} decrease the write errors and increase the write disturbances, there is a trade-off relationship between these two failures. Suppose that the standard deviations σ of r_S, r_H, r_N, r_{WL}, r_{BL}, and I_{TH} have the same value. This is because these standard deviations tend to be similar and because the calculation is a simplification. Higher values of σ will increase the

BER for the same V_{DD}.

The operation window between the write disturbances and write errors is defined as shown in Fig. 7.10. The minimum write voltage V_{DDmin} is determined when the BER of the write error F_{WRITE} is equal to the BER required to obtain a working memory chip. In the same manner, the maximum write voltage V_{DDmax} is determined when the BER of the write disturbance $F_{DISTURB}$ is equal to the specification. The operation window is defined as the difference between V_{DDmax} and V_{DDmin}. The operation window required in the product will be discussed in Section 8.3.2.

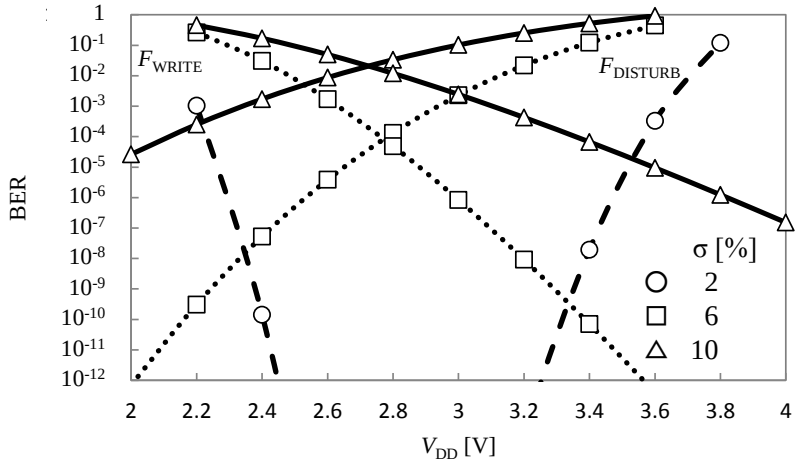


Fig. 7.8 BER in the V_{DD}/2 bias scheme during SET and RESET operations [24].

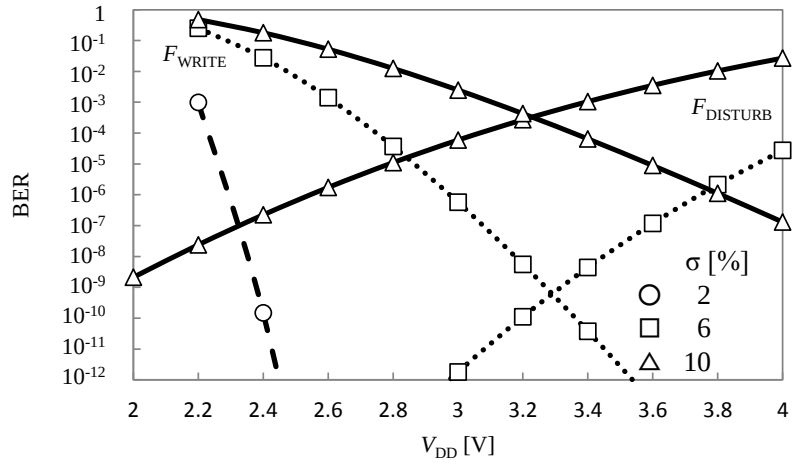


Fig. 7.9 BER in the V_{DD}/3 bias scheme during SET and RESET operations [24].

Table 7.3 Calculation parameters for estimating the write disturbances and write errors [24].

Parameter	Symbol	Value
Selected cell resistance in HRS	r_S	1×10^9 Ω
Selected cell resistance in LRS	r_S	1×10^8 Ω
WL half-selected cell resistance in HRS	r_R	1×10^9 Ω
WL half-selected cell resistance in LRS	r_R	1×10^8 Ω
BL half-selected cell resistance in HRS	r_C	1×10^9 Ω
BL half-selected cell resistance in LRS	r_C	1×10^8 Ω
Non-selected cell resistance with $V_{DD}/2$ scheme	r_N	1×10^{11} Ω
Non-selected cell resistance in HRS with $V_{DD}/3$ scheme	r_N	1×10^9 Ω
Non-selected cell resistance in LRS with $V_{DD}/3$ scheme	r_N	1×10^8 Ω
WL resistance	r_{WL}	4 Ω
BL resistance	r_{BL}	4 Ω
Selected WL voltage	V_{WL}	V_{DD}
Non-selected WL voltage with $V_{DD}/2$ scheme	V_{WL}	$V_{DD}/2$
Non-selected WL voltage with $V_{DD}/3$ scheme	V_{WL}	$V_{DD}/3$
Selected BL voltage	V_{BL}	0 V
Non-selected BL voltage with $V_{DD}/2$ scheme	V_{BL}	$V_{DD}/2$
Non-selected BL voltage with $V_{DD}/3$ scheme	V_{BL}	$2V_{DD}/3$
Number of WLs	m	512
Number of BLs	n	512
Threshold current for SET	I_{TH}	2 nA
Threshold current for RESET	I_{TH}	20 nA
Correlation efficient of I_{CELL} and I_{TH}	ρ	0

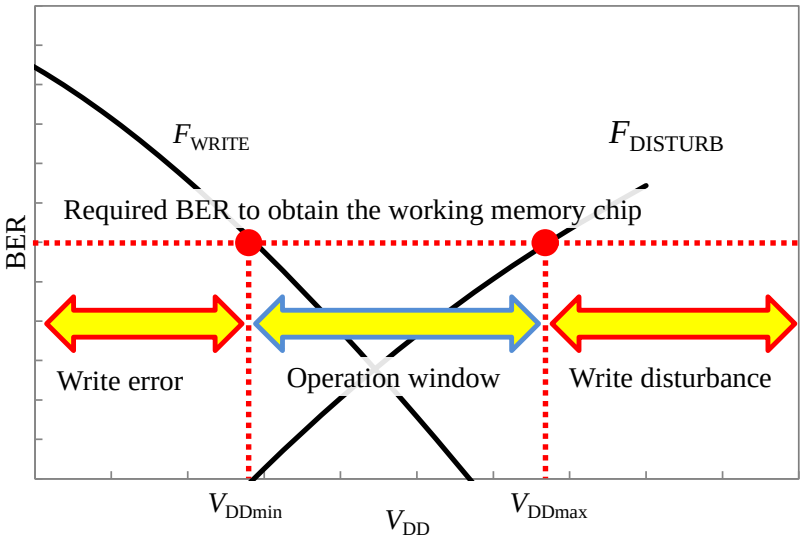


Fig. 7.10 Definition of operation window [24].

7.3 Summary

The read disturbances can be reduced by using a low read voltage. There are two bias schemes in the write cycle, namely the $V_{DD}/2$ scheme and the $V_{DD}/3$ scheme. The $V_{DD}/3$ scheme leads to larger operating margins than with the $V_{DD}/2$ scheme. This is because the applied voltage in the non-selected cell in the $V_{DD}/3$ scheme is less than that in the $V_{DD}/2$ scheme. However, as both cases produce large BERs, the current production line cannot provide any commercial products. In the next chapter, an ECC is applied to the cross-point array to rescue the failing bits produced by the trade-off relationship.

References

[35] J. Ai, X. Qi, W. Yu, Y, Deng, F. Liu, and L. Shi, "A new CFAR ship detection algorithm based on 2-D joint log-normal distribution in SAR images," IEEE Geoscience and Remote Sensing Letters, vol. 7, no. 4, pp. 806−810, 2010. doi: 10.1109/LGRS.2010.2048697.

Chapter 8 Reduction in the BER using error correcting code

8.1 Organization of Chapter 8

This chapter describes the application of ECCs to the cross-point memory with the aim of relaxing the BER produced by the trade-off relationship between the disturbances and write errors discussed in Chapter 7. ECCs are widely used for large-scale memories such as DRAM and NAND Flash to ensure a high yield and overcome errors during operation. This chapter is organized as follows.

First, the theory of ECCs is discussed in Section 8.2. The Hamming distance for the estimation of the number of correcting bits with ECCs is introduced in Subsection 8.2.1. One of the main purposes of Chapter 8 is to prepare the number of correcting bits with ECCs for the cross-point array. The fundamentals of Galois fields are then explained in Subsection 8.2.2, because the concepts are used to establish the ECCs. Furthermore, linear codes are explained in Subsection 8.2.3. The ECCs used for the semiconductor memory are derivatives of the linear code. The Hamming code, cyclic code, and Bose–Chaudhuri–Hocquenghem (BCH) code are introduced in Subsections 8.2.4, 8.2.5, and 8.2.6, respectively. Finally, by applying the BCH code to a 1 Gb memory with a cross-point array, it is demonstrated that the BER produced by the trade-off relationship between disturbances and write errors can be drastically relaxed in Section 8.3.

8.2 Error-correcting codes

8.2.1 Hamming distance

Let the code vectors $\boldsymbol{v} = (v_1, v_2, \cdots, v_n)$ and $\boldsymbol{w} = (w_1, w_2, \cdots, w_n)$ be chosen from a block code $\boldsymbol{C}$. The Hamming distance $d_H(\boldsymbol{v}, \boldsymbol{w})$ is defined as the number of elements for which $v_i \neq w_i$ for $i = 1, 2, \cdots, n$ [36]. The minimum distance in the linear code $\boldsymbol{C}$ [36] is defined as

$$d_{\min} = \min_{v,\, w \in C} \{d_H(v, w) \mid v \neq w\}. \qquad \text{Eq. 8.1}$$

The Hamming weight $W_H(\boldsymbol{w})$ is the number of nonzero elements in $\boldsymbol{w}$. The Hamming sphere is defined as a set that has a Hamming distance of less than or equal to t from $\boldsymbol{w}$ with code length n [36]. The sphere is expressed as

$$S_t(w) = \{x \mid d_H(w, x) \leq t\}, \qquad \text{Eq. 8.2}$$

where $\boldsymbol{x}$ is an n-dimensional vector. Suppose t bits in $\boldsymbol{w}$ fail after an operation. If the failed code vector is denoted as $\boldsymbol{v}$, the Hamming distance $d_H(\boldsymbol{w}, \boldsymbol{v})$ between $\boldsymbol{w}$ and $\boldsymbol{v}$ is t. Thus, the code vectors differing from $\boldsymbol{w}$ by t bits belong to $S_t(\boldsymbol{w})$ with a diameter of t. If $2t + 1 \leq d_{\min}$, t bits can be corrected in $\boldsymbol{w}$.

8.2.2 Galois fields

Galois field theory [36][38] plays an important role in the BCH code, which is discussed in Subsection 8.2.6. A Galois field is a set with a finite number of elements that obey the four basic arithmetic operations. The Galois field with q elements is represented by $GF(q)$ or F_q. When $q = 2$, that is, $GF(2) = \{0, 1\}$, addition and multiplication are defined as in Tables 8.2 and 8.3, respectively.

Table 8.1 Addition table of $GF(2)$.

+	0	1
0	0	1
1	1	0

Table 8.2 Multiplication table of $GF(2)$.

×	0	1
0	0	0
1	0	1

Let x be indeterminate. The polynomial in x with coefficients in a field F is expressed as

$$f(x) = a_n x^n + a_{n-1} x^{n-1} + \cdots + a_1 x + a_0, \qquad \text{Eq. 8.3}$$

where $a_n \neq 0$. The largest dimension n in $f(x)$ is the degree, denoted by *deg* f(x). If $f(x)$ over F cannot be divided by itself or by any polynomials except one, $f(x)$ is irreducible over F.

The Galois extension field [36] can be obtained by adding a root of the irreducible polynomial $f(x)$ over the Galois field to the Galois field. Let α be the root of the irreducible polynomial $f(x) = x^2 + x + 1$ over $GF(2)$. It is found that the set $G = \{0, 1, \alpha, \alpha^2\}$ forms a field (see Table 8.3 and Table 8.4). Because this is the Galois field with four elements, it is denoted by $GF(2^2)$ or $GF(4)$. $GF(2^2)$ is called the two-dimensional Galois extension field of $GF(2)$. Thus, the Galois extension field $GF(2^2)$ can be constructed using the root α of the irreducible polynomial $f(x) = x^2 + x + 1$.

Table 8.3 Addition table of $GF(2^2) = \{0, 1, \alpha, \alpha^2\}$.

+	0	1	α	α^2
0	0	1	α	α^2
1	1	0	α^2	α
α	α	α^2	0	1
α^2	α^2	α	1	0

Table 8.4 Multiplication table of $GF(2^2) = \{0, 1, \alpha, \alpha^2\}$.

×	0	1	α	α^2
0	0	0	0	0
1	0	1	α	α^2
α	0	α	α^2	1
α^2	0	α^2	1	α

The minimum integer n satisfying $\alpha^n = 1$ is called the order of α. When the root α of the m-dimensional polynomial $f(x)$ over $GF(2)$ is $2^m - 1$, $f(x)$ is the primitive polynomial.

Furthermore, the minimal polynomial is defined as the polynomial with root α and the minimum dimension over the Galois field. The m-dimensional Galois extension field of $GF(2)$ is denoted by

$$GF(2^m) = \{0, 1, \alpha, \alpha^2, \cdots, \alpha^{2^m-2}\}, \quad \text{Eq. 8.4}$$

where α is the primitive element over $GF(2^m)$. In accordance with the factor theorem, $x^{2^m} - x$ over $GF(2^m)$ can be factorized as

$$x^{2^m} - x = x(x-1)(x-\alpha)(x-\alpha^2)\cdots(x-\alpha^{2^m}). \quad \text{Eq. 8.5}$$

Thus, the roots of $x^{2^m} - x$ correspond to $GF(2^m) = \{0, 1, \alpha, \alpha^2, \cdots, \alpha^{2^m-2}\}$, where α is a primitive element and the order is $2^m - 1$. Table 8.5 presents an example of the primitive polynomials over $GF(2)$ for various m.

Table 8.5 Example of primitive polynomials over $GF(2)$ [36].

m	Primitive polynomial $f(x)$
1	$x + 1$
2	$x^2 + x + 1$
3	$x^3 + x + 1$
4	$x^4 + x + 1$
5	$x^5 + x^2 + 1$
6	$x^6 + x + 1$
7	$x^7 + x + 1$
8	$x^8 + x^6 + x^5 + x^4 + 1$
9	$x^9 + x^4 + 1$
10	$x^{10} + x^3 + 1$
11	$x^{11} + x^2 + 1$
12	$x^{12} + x^7 + x^4 + x^3 + 1$
13	$x^{13} + x^4 + x^3 + x + 1$
14	$x^{14} + x^{12} + x^{11} + x + 1$
15	$x^{15} + x + 1$
16	$x^{16} + x^5 + x^3 + x^2 + 1$
17	$x^{17} + x^3 + 1$
18	$x^{18} + x^7 + 1$
19	$x^{19} + x^6 + x^5 + x + 1$
20	$x^{20} + x^3 + 1$

Let a polynomial over *GF*(2) be

$$f(x) = a_n x^n + a_{n-1} x^{n-1} + \cdots + a_n x + a_0, \quad \text{Eq. 8.6}$$

where $a^n = 1$. Multiplying both sides of Eq. 8.6 by itself $s - 1$ times yields

$$f\left(x^{2^s}\right) = \left\{f(x)\right\}^{2^s}, \quad \text{Eq. 8.7}$$

where s is a positive integer. Let α and l be a nonzero element of *GF*(2) and the minimum positive integer satisfying

$$\alpha^{2^l} = \alpha, \quad \text{Eq. 8.8}$$

respectively. If α is a root of $f(x)$, then Eq. 8.7 implies that

$$f\left(\alpha^{2^s}\right) = \left\{f(\alpha)\right\}^{2^s} = 0, \quad \text{Eq. 8.9}$$

for $s = 1, 2, \cdots, l - 1$. Consequently, α^2, α^{2^2}, $\cdots$, and $\alpha^{2^{l-1}}$ are also roots of $f(x)$. These are called conjugate elements of α. If $f(x)$ is an l–dimensional monic polynomial with α, α^2, α^{2^2}, $\cdots$, and $\alpha^{2^{l-1}}$ as the roots, $f(x)$ is written as

$$f(x) = (x - \alpha)(x - \alpha^2)\left(x - \alpha^{2^2}\right)\cdots\left(x - \alpha^{2^{l-1}}\right). \quad \text{Eq. 8.10}$$

It is known that $f(x)$ is the minimal polynomial over *GF*(2) and that $f(x)$ is the minimal polynomial of α^2, α^{2^2}, $\cdots$, and $\alpha^{2^{l-1}}$.

8.2.3 Linear code

A block code is a set that consists of a series of code blocks. Each code block has information bits and parity bits. A code word is an element of the set and is expressed as an n-dimensional vector $\boldsymbol{w} = (w_1, w_2, w_3, \cdots, w_n)$ (or simply by $\boldsymbol{w} = w_1 w_2 w_3 \cdots w_n$). The total number of bits n in the code word is the code length. Thus, a code word consisting of k information bits and $n - k$ parity check bits, as shown in Fig. 8.1, is called the (n, k) code. The information bits are originally written by those who use the memory equipped with the code. If some of them

have failed, the parity check bits check the error.

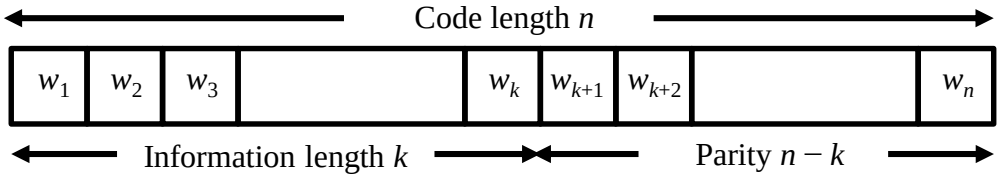


Fig. 8.1 (n, k) code with code length n and information length k [24].

Let two code words $\boldsymbol{v} = (v_1, v_2, \cdots, v_n)$ and $\boldsymbol{w} = (w_1, w_2, \cdots, w_n)$ be randomly chosen from a block code $\boldsymbol{C}$. If $\boldsymbol{v} + \boldsymbol{w}$ is a code word of $\boldsymbol{C}$, then $\boldsymbol{C}$ is a linear code. In the (n, k) linear code, the information vector with k bits can be transformed to the code vector with length n. Let the information and the code vectors be $\boldsymbol{a} = (a_1, a_2, \cdots, a_k)$ and $\boldsymbol{w} = (w_1, w_2, \cdots, w_n)$, respectively. The linear (n, k) code is generated by

$$w = aG, \qquad \text{Eq. 8.11}$$

where $\boldsymbol{G}$ is a generator matrix given by

$$G = \begin{pmatrix} g_{11} & g_{12} & \cdots & g_{1n} \\ g_{21} & g_{22} & \cdots & g_{2n} \\ & & \cdots & \\ g_{k1} & g_{k2} & \cdots & g_{kn} \end{pmatrix}. \qquad \text{Eq. 8.12}$$

The $n \times k$ matrix $\boldsymbol{G}$ can be transformed to an irreducible matrix $\boldsymbol{G}_0$ as

$$G_0 = (I_k \; P), \qquad \text{Eq. 8.13}$$

where $\boldsymbol{I}_k$ and $\boldsymbol{P}$ are the k-dimensional unit matrix and an $n - k$-dimensional matrix, respectively. The information vector $\boldsymbol{a} = (a_1, a_2, \cdots, a_k)$ is coded by $\boldsymbol{G}_0$ as

$$aG_0 = a(I_k \; P) = (a \; aP). \qquad \text{Eq. 8.14}$$

The code ($\boldsymbol{a}$, $\boldsymbol{aP}$) is an n-dimensional vector composed of the information and the parity vectors.

A parity check matrix $\boldsymbol{H}$ is defined as

$$GH^T = O, \quad \text{Eq. 8.15}$$

where $\boldsymbol{O}$ is the $k \times (n - k)$ zero matrix. Thus, $\boldsymbol{H}$ is an $(n - k) \times n$ matrix. Multiplying the information vector $\boldsymbol{a}$ by Eq. 8.15, a parity check equation is obtained as

$$wH^T = \mathbf{0} \quad \text{Eq. 8.16}$$

If the parity check matrix $\boldsymbol{H}$ is given, $\boldsymbol{w}$ generates linear codes with (n, k).

8.2.4 Hamming code

The Hamming code was introduced in 1950 [37]. It is an error-correcting linear code that has an $m \times (2^m - 1)$ parity check matrix composed of m-dimensional vectors. Note that the m-dimensional vectors are each distinct and nonzero. Thus, the number of row vectors is $2^m - 1$. The code length of the Hamming code is equal to the number of row vectors, i.e., $n = 2^m - 1$. Because the minimum distance $d_{\min}$ of the Hamming code is 3 [38], the Hamming code corrects errors as described in Subsection 8.2.1.

Let $\boldsymbol{w}$ be the code vector with code length $2^m - 1$. By inserting $\boldsymbol{w}$ in the parity check equation (Eq. 8.16), m equations are obtained. Thus, $2^m - 1 - m$ elements can be determined. The number of information bits k is $2^m - 1 - m$. Consequently, the Hamming code is the linear code that represents $(2^m - 1, 2^m - 1 - m, 3)$, where m is an integer that is greater than or equal to 2.

8.2.5 Cyclic code

The cyclic code is a linear block code that is widely used for digital equipment. The cyclic Hamming code, BCH code, and Reed–Solomon (RS) code are derived from the cyclic code. Let $\boldsymbol{w} = a_0 a_1 \cdots a_{n-2} a_{n-1}$ be a code word of length n in a linear code $\boldsymbol{C}$. If the code word $\boldsymbol{w}' = a_{n-1} a_0 \cdots a_{n-3} a_{n-2}$ in which each element of $\boldsymbol{w}$ is shifted to the right is a code word in $\boldsymbol{C}$, $\boldsymbol{C}$ is

a cyclic code. In a cyclic code $\boldsymbol{C}$ of length n, if $a_0a_1\cdots a_{n-2}a_{n-1} \in \boldsymbol{C}$, then $a_{n-1}a_0\cdots a_{n-3}a_{n-2} \in \boldsymbol{C}$.

The shift of elements in the cyclic code can be expressed by a polynomial. Let the code word $\boldsymbol{w} = a_0a_1\cdots a_{n-2}a_{n-1}$ be transformed to a code polynomial as

$$w(x) = a_0 + a_1x + \cdots + a_nx^{n-1}, \qquad \text{Eq. 8.17}$$

where x is indeterminate. The shifted $\boldsymbol{w}' = a_{n-1}a_0\cdots a_{n-3}a_{n-2}$ from $\boldsymbol{w} = a_0a_1\cdots a_{n-2}a_{n-1}$ can be obtained as the remainder after multiplying both sides of Eq. 8.17 by x and dividing by $x^n - 1$. Multiplying both sides of Eq. 8.17 by x yields

$$\begin{aligned} xw(x) &= a_0x + a_1x^2 + \cdots + a_{n-1}x^n \qquad \text{Eq. 8.18} \\ &= a_{n-1} + a_0x + a_1x^2 + \cdots + a_{n-2}x^{n-1} + a_{n-1}(x^n - 1). \end{aligned}$$

Dividing Eq. 8.18 by $x^n - 1$, the remainder is obtained as $a_{n-1} + a_0x + a_1x^2 + \cdots + a_{n-2}\,x^{n-1}$. It can be confirmed that $\boldsymbol{w}$ is shifted to $\boldsymbol{w}'$ by multiplying both sides of Eq. 8.17 by x and dividing them by $x^n - 1$. In a cyclic code $\boldsymbol{C}$, if $w(x) \in \boldsymbol{C}$, then $xw(x) \in \boldsymbol{C}$. Multiplying both sides of Eq. 8.17 by x l times, Eq. 8.18 can be generalized. Thus, in a cyclic code $\boldsymbol{C}$, if $w(x) \in \boldsymbol{C}$, then $x^lw(x) \in \boldsymbol{C}$.

Furthermore, it is known that a code polynomial $w(x)$ in a cyclic code $\boldsymbol{C}$ generates a code polynomial $a(x)w(x)$ in $\boldsymbol{C}$, where $a(x)$ is any polynomial. Thus, if $g(x)$ is a nonzero minimum code polynomial in $\boldsymbol{C}$, any code polynomial $w(x)$ in $\boldsymbol{C}$ can be written by

$$w(x) = a(x)g(x), \qquad \text{Eq. 8.19}$$

where $g(x)$ and $a(x)$ and are called a generator polynomial and an information polynomial, respectively. The (n, k) cyclic code of length n and number of information bits k has the generator polynomial and information polynomial

$$g(x) = g_0 + g_1x + \cdots + g_{n-k}x^{n-k}, \qquad \text{Eq. 8.20}$$

$$a(x) = a_0 + a_1x + \cdots + a_{k-1}x^{k-1}, \qquad \text{Eq. 8.21}$$

respectively. Here, $deg\ g(x) = n - k$ and $deg\ a(x) \leq k - 1$.

Eq. 8.19 can be written in vector form as

$$a(x)g(x) = (a_0, a_1, \cdots, a_{n-1}) \begin{pmatrix} g_0 & g_1 & g_2 & \cdots & g_{n-k} & 0 & \cdots & \cdots & 0 \\ 0 & g_0 & g_1 & g_2 & \cdots & g_{n-k} & 0 & \cdots & 0 \\ \vdots & \ddots & \ddots & \ddots & \ddots & \ddots & \ddots & \ddots & \vdots \\ 0 & \cdots & \cdots & 0 & g_0 & g_1 & g_2 & \cdots & g_{n-k} \end{pmatrix}. \quad \text{Eq. 8.22}$$

The $k \times n$ matrix in Eq. 8.22 is a generator matrix in a cyclic code. It is known that g(x) divides $x^n - 1$. Thus, a parity check polynomial $h(x)$ is defined as

$$h(x) = \frac{x^n - 1}{g(x)} = h_k x^k + \cdots + h_1 x + h_k. \quad \text{Eq. 8.23}$$

Using $h(x)$, a parity check matrix $\boldsymbol{H}$ is obtained as

$$\boldsymbol{H} = \begin{pmatrix} 0 & \cdots & \cdots & 0 & h_k & h_{k-1} & \cdots & h_0 \\ 0 & \cdots & 0 & h_k & h_{k-1} & \cdots & h_0 & 0 \\ \vdots & \iddots & \iddots & \iddots & \iddots & \iddots & \iddots & \vdots \\ h_k & h_{k-1} & \cdots & h_0 & 00 & \cdots & \cdots & 0 \end{pmatrix}, \quad \text{Eq. 8.24}$$

where $\boldsymbol{G}\boldsymbol{H}^T = \boldsymbol{O}$. It is known that $g(x)$ generates an $(n, k, 3)$ cyclic Hamming code when $g(x)$ is the m-dimensional primitive polynomial.

8.2.6 Bose–Chaudhuri–Hocquenghem code

The BCH code [39][40] is derived from the cyclic Hamming code and features multiple error correction and simple coding and decoding. Thus, it is widely used for large-scale semiconductor memories.

From Subsection 8.2.5, when $g(x)$ is an m-dimensional primitive polynomial, $g(x)$ generates the $(n, k, 3)$ cyclic Hamming code. Here, $n = 2^m - 1$ and $k = n - m$. From Subsection 8.2.2, a root α of $g(x)$ is a primitive element over $GF(2^m)$. A code word $w(x) = a(x)g(x)$ of a cyclic code can be written as

$$w(x) = w_0 + w_1 \mathrm{x} + \cdots + w_{n-1} x^{n-1}. \quad \text{Eq. 8.25}$$

Substituting α into Eq. 8.25 leads to

$$wH^T = O, \quad \text{Eq. 8.26}$$

where the code vector $\boldsymbol{w}$ and the parity check matrix $\boldsymbol{H}$ of the Hamming code are

$$\boldsymbol{w} = (w_0, w_1, \cdots, w_{n-1}), \quad \text{Eq. 8.27}$$

$$\boldsymbol{H} = \begin{pmatrix} 1 & 0 & 0 & \cdots & \cdots & \cdots & \cdots & \cdots \\ 0 & 1 & 0 & \cdots & \cdots & \cdots & \cdots & \cdots \\ 0 & 0 & 1 & \cdots & \cdots & \cdots & \cdots & \cdots \\ \vdots & \vdots & \vdots & \cdots & \cdots & \cdots & \cdots & \cdots \\ 0 & 0 & 0 & \cdots & \cdots & \cdots & \cdots & \cdots \end{pmatrix}, \quad \text{Eq. 8.28}$$

respectively. $\boldsymbol{H}$ is an $m \times 2^m - 1$ matrix. The matrix expression is used for $\boldsymbol{H}$.

The definition of the BCH code is described as follows. Let α be a primitive element over $GF(2^m)$. Furthermore, let $M_h(x)$ be a minimal polynomial of α^h for $h = 1, 2, \cdots, 2t$, where t is a positive integer. Here, $2t \leq 2^m - 1$. The BCH code is a cyclic code for which the generator polynomial is

$$g(x) = \text{LCM}\{M_1(x), M_2(x), \cdots, M_{2t}(x)\}, \quad \text{Eq. 8.29}$$

where LCM denotes the least common multiple. The code length n is a divisor of $2^m - 1$. When $n = 2^m - 1$, the BCH code is called the primitive BCH code. If $t = 1$, the BCH code becomes the cyclic Hamming code. As the series of roots $\alpha, \alpha^2, \cdots,$ and α^{2t} are involved in the roots of $g(x)$, the minimum distance $d_{\min}$ is greater than $2t + 1$. Thus, the BCH code can correct t errors. It is said that $d = 2t + 1$ is the designed distance of the BCH code. The number of information bits k is given by $k = n - deg\ g(x)$. Therefore, if the information polynomial $a(x)$ is given by $a(x) = a_0 + a_1x + \cdots + a_{k-1}x^{k-1}$, the (n, k) BCH code is obtained from $w(x) = a(x)g(x)$.

Here, the generator polynomial $g(x)$, number of information bits k, and designed distance d are calculated for a BCH code of length $n = 63$ in order to apply the BCH code to the 1 Gb memory in Subsection 8.3.2.

Let α be a primitive element over $GF(2^m)$, where $n = 63$. Because $n = 2^m - 1$, we have that $m = 6$. First, the minimal polynomials of the series of roots $\alpha, \alpha^2, \cdots,$ and α^{2t} are introduced to obtain $g(x)$, as explained in Eq. 8.29. As mentioned in Table 8.5, the primitive polynomial with $m = 6$ over $GF(2)$ is $M_1(x) = x^6 + x + 1$. In accordance with the factor theorem, $x^{64} - x$ is

factorized as

$$x^{64} - x = x(x+1)(x^6 + x + 1)(x^6 + x^4 + x^2 + x + 1) \quad \text{Eq. 8.30}$$
$$(x^6 + x^5 + x^2 + x + 1)(x^6 + x^3 + 1)(x^3 + x^2 + 1)$$
$$(x^6 + x^5 + x^3 + x^2 + 1)(x^6 + x^4 + x^3 + x + 1)$$
$$(x^6 + x^5 + x^4 + x^2 + 1)(x^2 + x + 1)$$
$$(x^6 + x^5 + x^4 + x + 1)(x^3 + x + 1)(x^6 + x^5 + 1),$$

where the roots of x and $x + 1$ are 0 and 1, respectively. The roots of the other factors correspond to the conjugate elements of the minimal polynomials summarized in Table 8.6. For instance, let us confirm that $M_3(\alpha^3) = 0$. Substituting $x = \alpha^3$ into $M_3(x)$ leads to $(\alpha^3)^6 + (\alpha^3)^4 + (\alpha^3)^2 + \alpha^3 + 1 = (\alpha^6)^3 + (\alpha^6)^2 + \alpha^6 + \alpha^3 + 1$. As $M_1(\alpha) = \alpha^6 + \alpha + 1 = 0$, $\alpha^6 = \alpha + 1$. In accordance with Tables 8.3 and 8.4, $M_3(\alpha^3)$ becomes $(\alpha + 1)^3 + (\alpha + 1)^2 + \alpha + 1 + \alpha^3 + 1 = (1 + 1)\alpha^3 + (1 + 1 + 1 + 1)\alpha^2 + (1 + 1 + 1 + 1 + 1 + 1)\alpha + 1 + 1 + 1 + 1 = 0$. Consequently, it is confirmed that $x = \alpha^3$ is a root of $M_3(x)$.

Table 8.6 Conjugate elements and minimal polynomials over $GF(2^6)$.

Conjugate element	Minimal polynomial
$\alpha, \alpha^2, \alpha^4, \alpha^8, \alpha^{16}, \alpha^{32}$	$M_1(x) = x^6 + x + 1$
$\alpha^3, \alpha^6, \alpha^{12}, \alpha^{24}, \alpha^{48}, \alpha^{96} = \alpha^{33}$	$M_3(x) = x^6 + x^4 + x^2 + x + 1$
$\alpha^5, \alpha^{10}, \alpha^{20}, \alpha^{40}, \alpha^{80} = \alpha^{17}, \alpha^{34}$	$M_5(x) = x^6 + x^5 + x^2 + x + 1$
$\alpha^7, \alpha^{14}, \alpha^{28}, \alpha^{56}, \alpha^{112} = \alpha^{49}, \alpha^{98} = \alpha^{35}$	$M_7(x) = x^6 + x^3 + 1$
$\alpha^9, \alpha^{18}, \alpha^{36}$	$M_9(x) = x^3 + x^2 + 1$
$\alpha^{11}, \alpha^{22}, \alpha^{44}, \alpha^{88} = \alpha^{25}, \alpha^{50}, \alpha^{100} = \alpha^{37}$	$M_{11}(x) = x^6 + x^5 + x^3 + x^2 + 1$
$\alpha^{13}, \alpha^{26}, \alpha^{52}, \alpha^{104} = \alpha^{41}, \alpha^{82} = \alpha^{19}, \alpha^{38}$	$M_{13}(x) = x^6 + x^4 + x^3 + x + 1$
$\alpha^{15}, \alpha^{30}, \alpha^{60}, \alpha^{120} = \alpha^{57}, \alpha^{114} = \alpha^{51}, \alpha^{102} = \alpha^{39}$	$M_{15}(x) = x^6 + x^5 + x^4 + x^2 + 1$
α^{21}, α^{42}	$M_{21}(x) = x^2 + x + 1$
$\alpha^{23}, \alpha^{46}, \alpha^{92} = \alpha^{29}, \alpha^{58}, \alpha^{116} = \alpha^{53}, \alpha^{106} = \alpha^{43}$	$M_{23}(x) = x^6 + x^5 + x^4 + x + 1$
$\alpha^{27}, \alpha^{54}, \alpha^{108} = \alpha^{45}$	$M_{27}(x) = x^3 + x + 1$
$\alpha^{31}, \alpha^{62}, \alpha^{124} = \alpha^{61}, \alpha^{122} = \alpha^{59}, \alpha^{118} = \alpha^{55}, \alpha^{110} = \alpha^{47}$	$M_{31}(x) = x^6 + x^5 + 1$

When $t = 1$, Eq. 8.29 implies that the generator polynomial $g(x)$ is given by

$$g(x) = \mathrm{LCM}\{M_1(x), M_2(x)\}. \quad \text{Eq. 8.31}$$

Because α and α^2 are conjugates, $M_1(x)$ and $M_2(x)$ are identical. Thus, Eq. 8.31 simply becomes

$$g(x) = M_1(x). \qquad \text{Eq. 8.32}$$

Thus, because $n - k = deg\ g(x) = 6$, we have that $k = 57$ and $d = 2t + 1 = 3$.

When $t = 2$, from Eq. 8.29, $g(x)$ is given by

$$g(x) = \mathrm{LCM}\{M_1(x), M_2(x), M_3(x), M_4(x)\} = M_1(x)M_3(x). \qquad \text{Eq. 8.33}$$

As $n - k = deg\ g(x) = 12$ from Table 8.6, we have $k = 51$ and $d = 2t + 1 = 5$.

In the same manner, the number of error correcting bits t and information length k can be calculated as in Table 8.7.

Table 8.7 Number of error correcting bits t and information length k over $GF(2^6)$.

t	k
1	57
2	51
3	45
4	39
5	36
6	30
7	24
10	18
11	16
13	10
15	7

8.3 Application of BCH code to 1 Gb memory

8.3.1 Yield model of semiconductor memories

The ECC with code length n and information length k is introduced for a 1 Gb memory, as illustrated in Fig. 8.1, where some errors in the k bits can be corrected by $n - k$ parity bits. Let g be the number of bits in the 1 Gb memory, including parity bits. If the BER is denoted by λ, the number of code and failing bits in the 1 Gb memory will be g/n and $g\lambda$, respectively. When $g\lambda$ failing bits are distributed randomly among g/n codes, the probability that a given code contains f failing bits is given by the binominal distribution [24][41][42]

$$P(f) = {}_{g\lambda}C_f \left(\frac{n}{g}\right)^f \left(1 - \frac{n}{g}\right)^{g\lambda - f} . \qquad \text{Eq. 8.34}$$

Note that the term ${}_{g\lambda}C_f$ in Eq. 8.34 cannot be calculated if $g\lambda$ is above some threshold. Thus, the next approximation is used in this study. When $g\lambda$ is large and $n\lambda$ remains finite, the binomial distribution Eq. 8.34 can be approximated by the Poisson distribution [24][41]

$$P(f) = \frac{n^f \lambda^f}{f!} \exp(-n\lambda). \qquad \text{Eq. 8.35}$$

Because the ECC corrects t out of n bits, the failure rate $F_{\mathrm{ECC}}(t, \lambda)$ that the ECC does not correct is given by [24][41]

$$F_{\mathrm{ECC}}(t, \lambda) = 1 - \sum_{f=0}^{t} P(f) . \qquad \text{Eq. 8.36}$$

Equation 8.36 is plotted in terms of the number of correcting bits t and the BER λ in Fig. 8.2. It is clear that the failure rate $F_{\mathrm{ECC}}(t, \lambda)$ is improved by using a large value of t.

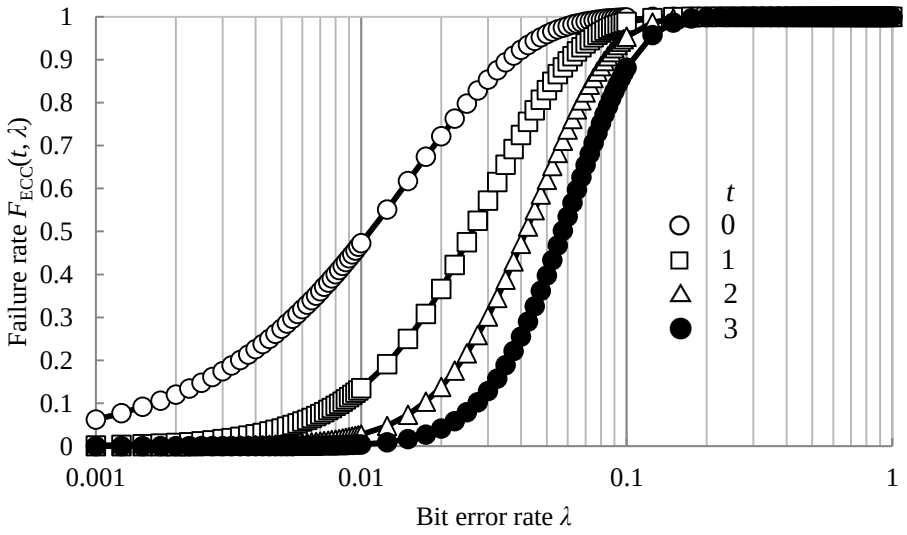


Fig. 8.2 Failure rate with respect to the number of correcting bits t and BER λ.

8.3.2 Yield enhancement by applying ECC to cross-point array memories

If the BCH code of length n = 64 is used for a 1 Gb memory, k and g will be obtained for t = 0, 1, ⋯, 7 as summarized in Table 8.8. The relationship between t and k is based on Table 8.7. The required $F_{\mathrm{ECC}}(t, \lambda)$ for obtaining the 1 Gb memory is defined as [24]

$$F_{\mathrm{ECC}}(t, \lambda) \leq \frac{n}{g}. \qquad \text{Eq. 8.37}$$

Let λ_{SPEC} be the required BER for realizing the 1 Gb memory. Here, it is assumed that half of λ_{BER} is assigned for write disturbances and half for write errors, i.e. [24],

$$F_{\mathrm{DISTURB}} \leq \frac{\lambda_{\mathrm{SPEC}}}{2}, \qquad \text{Eq. 8.38}$$

$$F_{\mathrm{WRITE}} \leq \frac{\lambda_{\mathrm{SPEC}}}{2}. \qquad \text{Eq. 8.39}$$

Table 8.8 BCH code of length n = 64 for the 1 Gb memory [24].

Number of correcting bits t	Information length k	Total number of bits g
0	64	1,073,741,824
1	57	1,205,604,856
2	51	1,347,440,721
3	45	1,527,099,484
4	39	1,762,037,866
5	36	1,908,874,354
6	30	2,290,649,225
7	24	2,863,311,531

For the ECC defined in the previous section and a 1 Gb memory chip with the $V_{\mathrm{DD}}/2$ and the $V_{\mathrm{DD}}/3$ bias schemes, the respective operation windows are shown in Figs. 8.3 and 8.4, where the standard deviation σ of r_{S}, r_{R}, r_{C}, r_{N}, r_{WL}, r_{BL}, and I_{TH} are parameters. They have the same value and are normalized with respect to their expectations. This calculation was conducted under the conditions of Table 7.3.

When t = 0, σ with the $V_{\mathrm{DD}}/2$ and the $V_{\mathrm{DD}}/3$ bias schemes should be less than 1% and

4%, respectively, to obtain operation windows of 1 V. These σ values are critical for the production line.

However, using the $V_{DD}/3$ bias scheme and the ECC with $t = 4$, the operation window can take a larger value. The ECC with $t = 4$ has been used in NAND Flash memory [42]. The 1Gb memory with σ in the $V_{DD}/2$ and $V_{DD}/3$ bias schemes can be relaxed to be less than 3% and 7%, respectively. The latter matches the production line. Therefore, the 1 Gb memory composed of cross-point arrays has an operation margin that matches the production line under the $V_{DD}/3$ scheme and the ECC with $t = 4$.

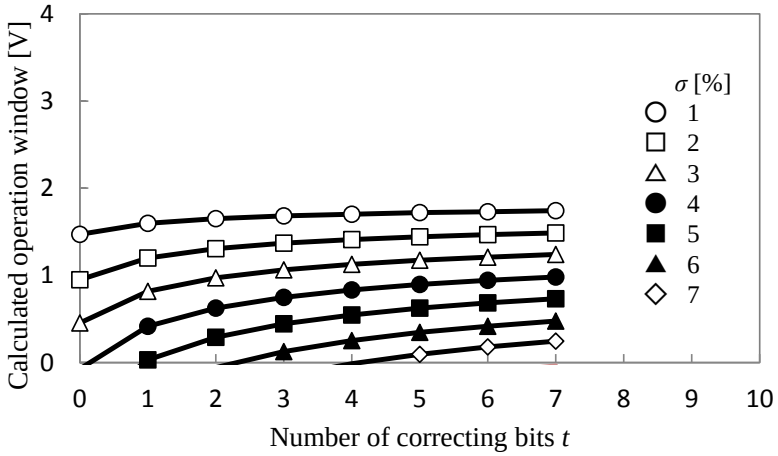


Fig. 8.3 Operation window of the 1 Gb memory in the $V_{DD}/2$ bias scheme [24].

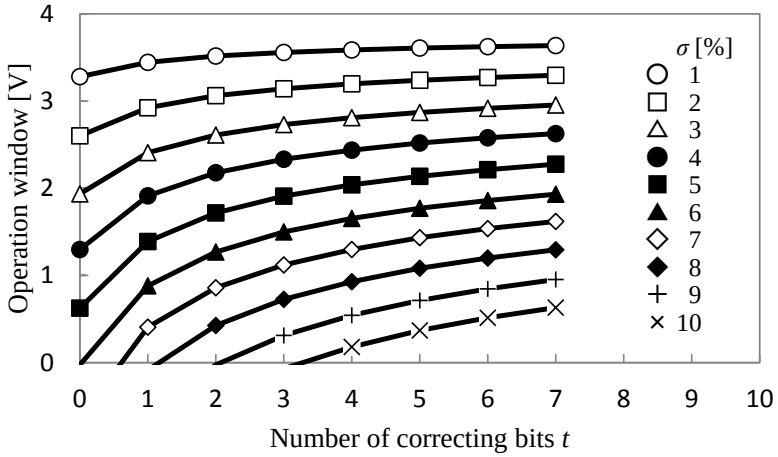


Fig. 8.4 Operation window of the 1 Gb memory in the $V_{DD}/3$ bias scheme [24].

8.4 Summary

The new simplified circuits were applied to estimate the BER of write disturbances in the cross-point array memory. The trade-off relationship between the write disturbances and write errors was estimated as a function of the write voltage in both the $V_{DD}/2$ and $V_{DD}/3$ schemes. It was found that the 1 Gb memory had a sufficient operation margin under the $V_{DD}/3$ scheme and the ECC with $t = 4$. The proposed simplified circuits constitute a comprehensive tool for developing low-cost memory chips matching the current production lines.

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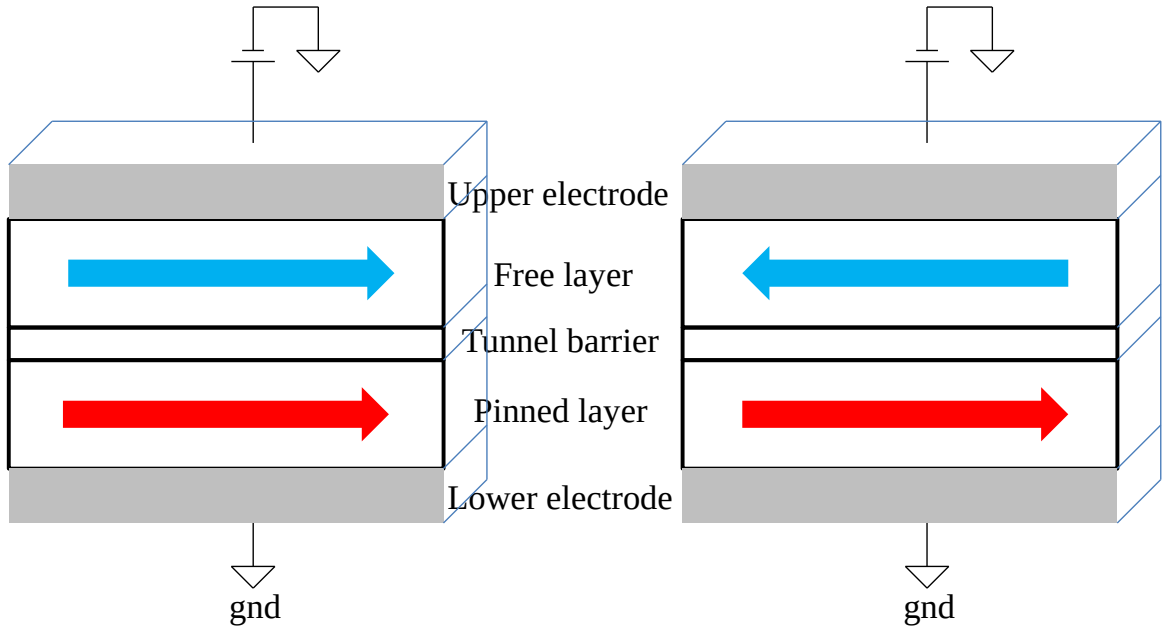
Chapter 9 Device design of MRAM

9.1 Operation of MRAM

Since MRAM as well as ReRAM is composed of cross-point arrays, disturbances can occur at the half-selected address while a datum is being written to the selected address. There is a trade-off relationship between the disturbance and the write error. Thus, the BER due to this trade-off relationship can be estimated by the models proposed for ReRAM. However, MRAM and ReRAM have different device parameters that affect the trade-off relationship. The effect of the device parameters on the operation window is investigated in this chapter.

MRAM is a non-volatile memory that uses the tunnel magnetoresistance (TMR) effect[32] [43][44]. Data are stored in magnetic tunnel junctions (MTJs), where a tunnel barrier is sandwiched by two ferromagnetic films. One is called the free layer and has a spin with two directions. The other is called the pinned layer and has a spin with one direction. Note that the spins tend to be located along the longer direction of the MTJ.

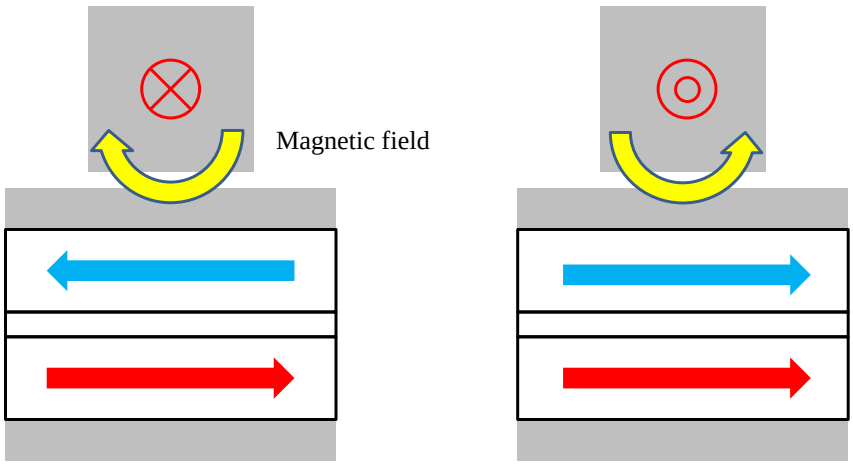
Corresponding to these two spins, MTJs have two resistance states, namely the low resistance state and high resistance state. When two spins are in parallel, MTJs exhibit low resistance, as shown in Fig. 9.1 (a). Here, some voltage is applied on the two electrodes. When two spins are anti-parallel, MTJs exhibit high resistance, as shown in Fig. 9.1 (b).



(a) Low resistance (Parallel-state) (b) High resistance (Anti-parallel-state)

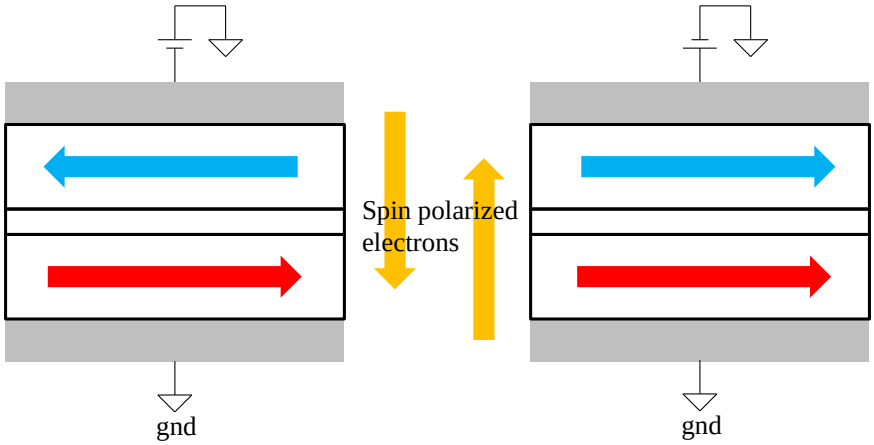
Fig. 9.1 Cross-sectional views of an MTJ.

From the viewpoint of writing data, there are two categories in MRAM. One utilizes the current induced magnetic field in order to flip the spin in the free layer [45][46][47][48]. Writing data is accomplished by changing the current direction as shown in Fig. 9.2. The current induced magnetic field is generated from a metal wire located over the MTJ. The second category utilizes the spin polarized electrons injected from the electrode [49][50][51][52][53][54]. Writing data is accomplished by changing the current direction as shown in Fig. 9.3. The spin in the free layer can be flipped with the injected spin polarized electrons. To distinguish these two MRAMs, the former is simply called MRAM and the latter is called spin torque transfer MRAM (STT-MRAM).



(a) Writing to high resistance state. (b) Writing to low resistance state.

Fig. 9.2 Writing data by current induced magnetic field.



(a) Writing to high resistance state. (b) Writing to low resistance state.

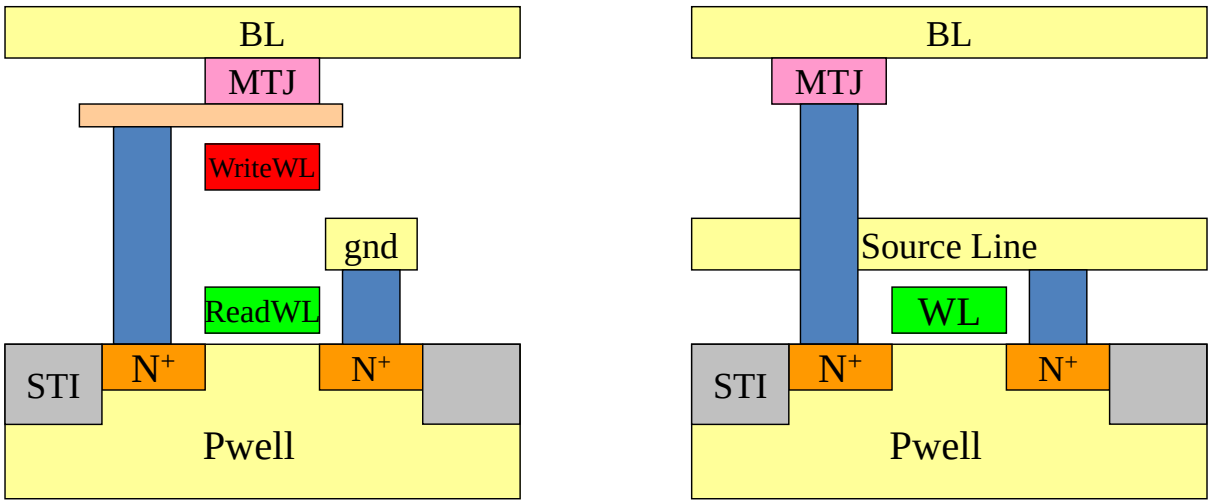
Fig. 9.3 Writing data by injecting spin polarized electrons.

9.2 Memory cell structure of MRAMs

Figure 9.4 (a) and (b) illustrate memory cells of MRAM and STT-MRAM, respectively. The memory cell of MRAM is composed of a BL, a write WL, an MTJ, and a metal oxide semiconductor field effect transistor (MOSFET)[33]. Data can be switched from the BL and the WL by the combined current induced magnetic field. The stored data is read out through the MOSFET. The memory cell of STT-MRAM is composed of a BL, an MTJ, and a MOSFET.

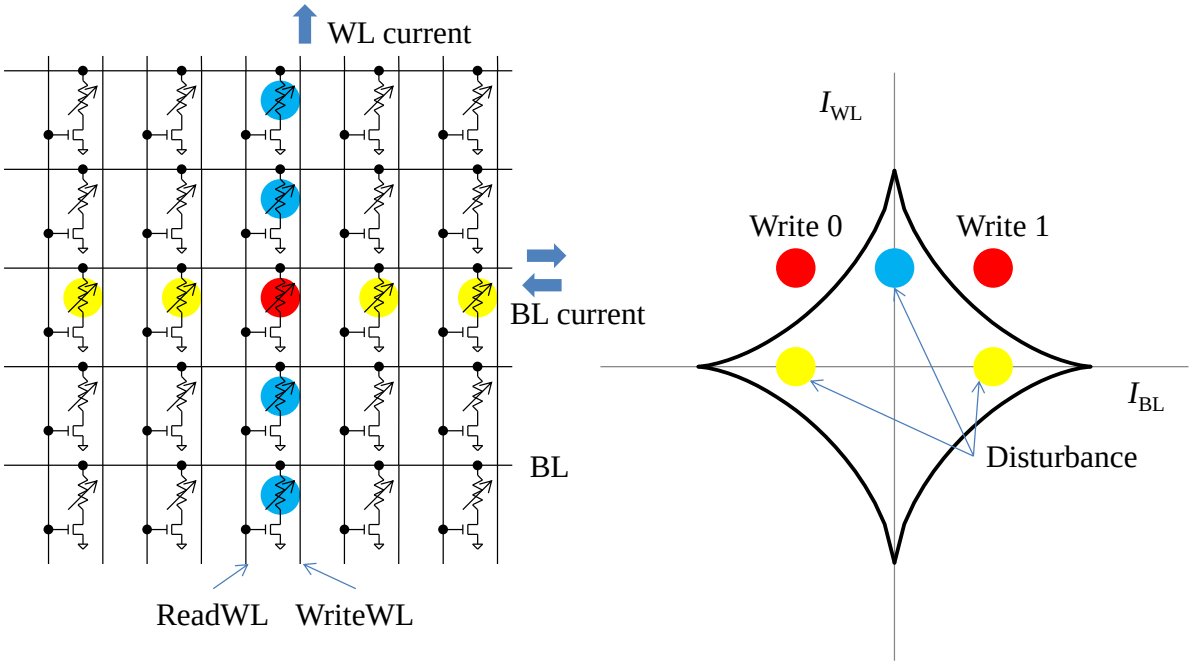
As STT-MRAM has no Write WL, it is more advantageous to large-scale memory than MRAM.

In this study, the operation window of MRAM is investigated because there is an important analogy with ReRAM: MRAM is also composed of cross-point memory. An equivalent MRAM circuit is illustrated in Fig. 9.5 (a), consisting of five BLs, five Read WLs, five Write WLs, and 25 MTJs. The MTJ in red is selected. The MTJs in blue and in yellow are half-selected by the Write WL and the BL, respectively. As data is switched by combined current induced magnetic field from the BL and WL, the threshold current can be expressed by two-dimensional curves of BL current (I_{BL}) and WL current (I_{WL}), as shown in Fig. 9.5 (b). When both I_{BL} and I_{WL} exceed the curves, data can be switched as indicated by red circles. The half-selected disturbance occurs in the blue and yellow circles. Thus, there is analogy with the cross-point array in terms of the trade-off relationship between the half-selected disturbance and the write error. Note that STT-MRAM has no half-selected disturbance because of its one transistor–one resistor (1T-1R) cell.



(a) MRAM (b) STT-MRAM

Fig. 9.4 Memory cells of MRAM and STT-MRAM.



(a) Equivalent circuit of MRAM (b) Asteroid curve

Fig. 9.5 Half-selected disturbance.

9.3 Trade-off relationship between half-selected disturbance and write error in MRAM

In this section, the operation window of MRAM is investigated by taking account of the half-selected disturbance. Suppose that the asteroid curve is symmetrical about I_{BL} and I_{WL} and about I_{BL} and $-I_{BL}$, as shown in Fig. 9.6. Let I_{TH} be the switching threshold current when $I_{BL} = I_{WL}$. Here, I_{WRITE} is defined as I_{BL} and I_{WL}. If I_{WRITE} does not exceed I_{TH}, a write error occurs. Furthermore, let I_{TH}^{H} be the switching threshold current when either I_{BL} or I_{WL} is zero. If I_{WRITE} exceeds I_{TH}^{H}, the half-selected disturbance occurs. I_{WRITE}, I_{TH}, and I_{TH}^{H} are distributed across the memory array. The relationship between these currents is illustrated in Fig. 9.7.

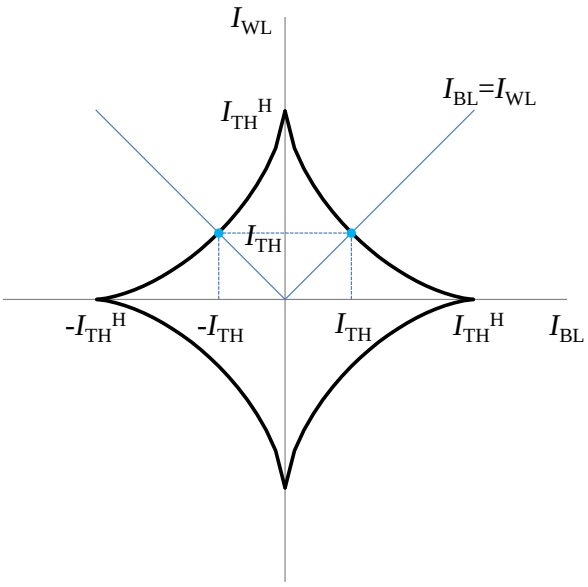


Fig. 9.6 Definition of I_{TH} and I_{TH}^{H} [48].

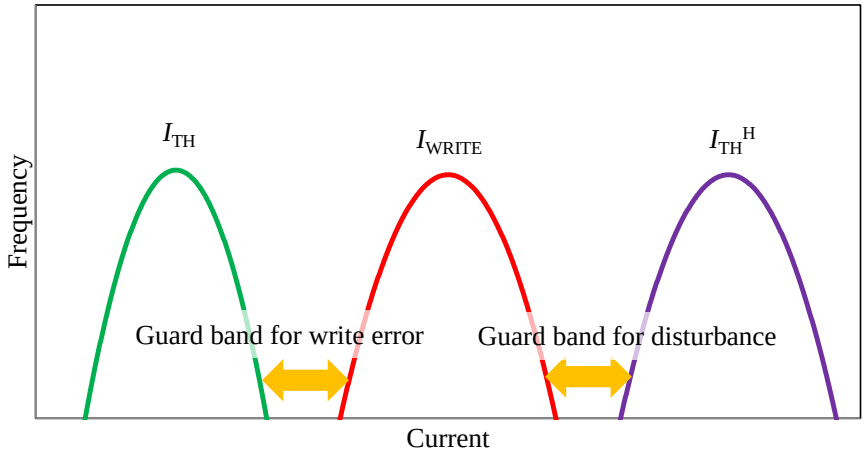


Fig. 9.7 Frequency curves of I_{TH}, I_{WRITE}, and I_{TH}^{H}.

The data switching probability P_{SW} is induced by the Sharrok formula [51][52][55]

$$P_{SW} = 1 - \exp\left\{-t_p f \exp\left[-\alpha\left(1-\frac{I_{WRITE}}{I_{TH}}\right)^2\right]\right\}. \quad \text{Eq. 9.1}$$

Here, I_{WRITE} is the current that generates an induced magnetic field using the pulse duration of t_P. Note that I_{WRITE} is defined such that $I_{WRITE} = I_{WL} = I_{BL}$, as mentioned in Fig. 9.6. f is an

attempt frequency of order 10^9 Hz. α is a thermal stability factor. When $I_{WRITE} = I_{TH}$, P_{SW} attains its maximum value. Thus, the failure rate can be estimated by comparing I_{TH} with I_{WRITE}.

The BER resulting from the half-selected disturbance and write error can be estimated in the same manner as in Section 3.2. Each MTJ has its own I_{TH}, I_{TH}^{H}, and I_{WRITE}. These currents are distributed across the array, and can be expressed by a two-dimensional function. Let $f(x, y)$ be the joint probability density function of the switching threshold current x and the write current y. If these currents obey the normal distribution, $f(x, y)$ is given by the bivariate normal distribution

$$f(x,y) = \frac{1}{2\pi\sigma_x\sigma_y\sqrt{1-\rho^2}} \mathrm{e}^{-\frac{1}{2(1-\rho^2)}\left[\frac{(x-\mu_x)^2}{\sigma_x^2} - \frac{2\rho(x-\mu_x)(y-\mu_y)}{\sigma_x\sigma_y} + \frac{(y-\mu_y)^2}{\sigma_y^2}\right]}, \quad \text{Eq. 9.2}$$

where μ_x, σ_x, μ_y, σ_y, and ρ denote the expectation of x, standard deviation of x, expectation of y, standard deviation of y, and correlation coefficient of x and y, respectively.

If I_{WRITE} exceeds I_{TH}^{H}, a disturbance occurs. By integrating over the region in which x is larger than y, the disturbance probability $F_{DISTURB}$ can be obtained as [23][24][26]

$$F_{DISTURB} = \int_0^\infty \int_0^y f(x,y)dxdy. \quad \text{Eq. 9.3}$$

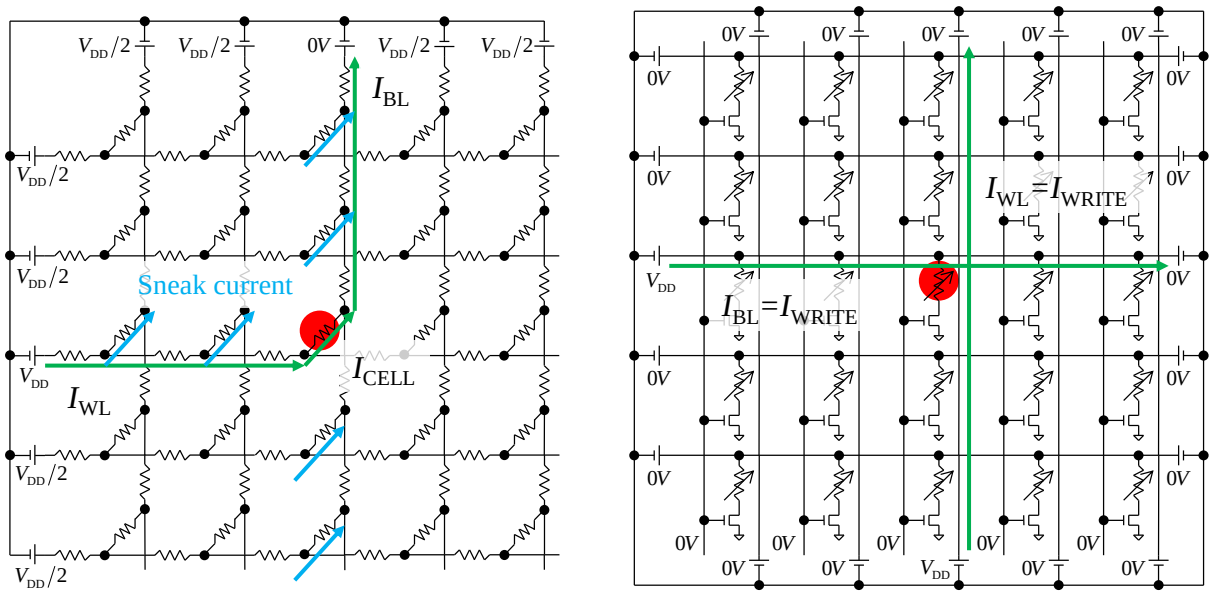
In the same manner, if I_{WRITE} is less than I_{TH}, a write error occurs. The write error probability F_{WRITE} is expressed by [23][24][26]

$$F_{WRITE} = \int_0^\infty \int_y^\infty f(x,y)dxdy. \quad \text{Eq. 9.4}$$

Eqs. 9.2, 9.3, and 9.4 are derived from Eqs. 3.1, 3.2 and 3.3, respectively. This is because the BER resulting from the half-selected disturbance and the write error can be estimated in the same manner as described in Section 3.2. Note that Eqs. 3.2 and 3.3 compare I_{TH} with I_{CELL} for ReRAM and that Eqs. 9.3 and 9.4 compare I_{TH} and I_{TH}^{H} with I_{WRITE} for MRAM.

There is a difference in the manner in which I_{CELL} and I_{WRITE} are treated. In the cross-

point array applied to ReRAM, the current supplied by the voltage source flows through the WL, the memory element, and the BL, as shown in Fig. 9.8 (a). In addition, the sneak current flows through the half- and the non-selected cells, as illustrated in Fig. 4.2. Thus, I_{CELL} can be obtained from Kirchhoff's laws as described in Section 2.4. However, the cross-point array applied to MRAM is simpler than that of ReRAM, as shown in Fig. 9.8 (b). As the MOSFET turns off during the write cycle, the write current only flows through the wire. I_{WRITE} is independent of the memory element resistance. Thus, the failure rate can be calculated by using I_{WRITE} tuned with the voltage source. Consequently, there is a difference in the calculation of BER between ReRAM and MRAM.



(a) ReRAM array (b) MRAM array

Fig. 9.8 Write current path in the cross-point arrays.

9.4 Simulation results

Using the BCH code of length n = 64 defined in Section 8.3, the respective operation windows are calculated for a 1 Gb MRAM. The operation window between the half-selected

disturbances and the write errors is defined as shown in Fig. 9.9. The minimum I_{WRITE} is determined when the BER of the write error $F_{WRITEmin}$ is equal to the BER required to obtain a working memory chip. In the same manner, the maximum $I_{WRITEmax}$ is determined when the BER of the write disturbance $F_{DISTURB}$ is equal to the specification. The operation window is defined as the difference between $I_{WRITEmax}$ and $I_{WRITEmin}$.

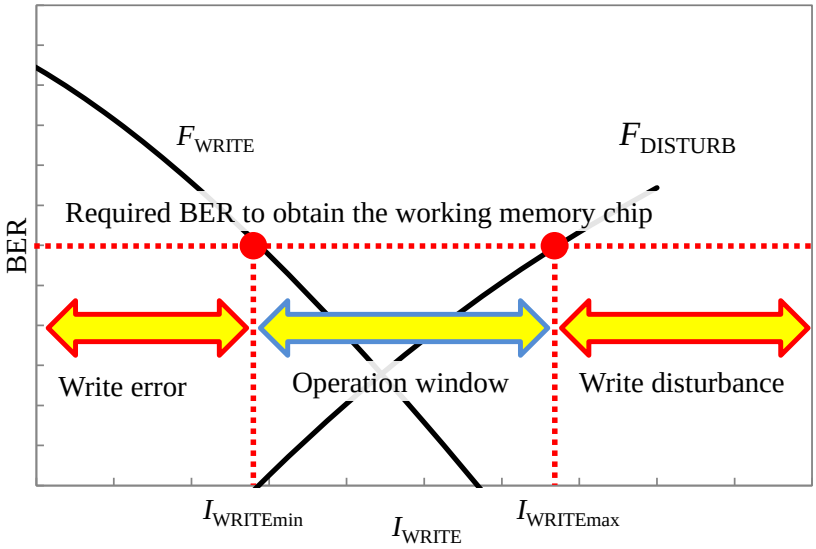


Fig. 9.9 Definition of operation window [24].

The operation windows are calculated as a function of the ratio of I_{TH} to I_{TH}^{H} (I_{TH}/I_{TH}^{H}). It is known that the operation windows increase as this ratio decreases. Thus, several studies have attempted to decrease the ratio [48][55][56][57][58][59]. Figures 9.10, 9.11, 9.12, 9.13 and 9.14 show the operation windows calculated with ratios of 0.1, 0.2, 0.3, 0.4, and 0.5, respectively. The standard deviation σ is that of I_{WRITE}, I_{TH}, and I_{TH}^{H}. They have the same value and are normalized with respect to their expectations.

Using Eqs. 9.3 and 9.4, the BER is estimated to be 0.0003 when $I_{TH}/I_{TH}^{H} = 0.3$ and $\sigma = 10\%$, while experimental results in 1Kb MRAM also demonstrated that there exists the trade-off relationship between disturbance and write error, and the resultant operation window

suggested the BER can be less than 0.0001 [48]. It indicates that the simulation models proposed in this thesis an estimate the BER caused by the trade-off relationship in MRAM.

Here, the same ECC scheme as for the 1 Gb ReRAM is applied to the 1 Gb MRAM, i.e., BCH code of length $n = 64$ with $t = 4$ correcting bits, as discussed in Section 8.3. Table 9.1 summarizes the minimum σ that ensures a nonzero operation window with $\sigma = 10\%$ for each I_{TH}/I_{TH}^{H}. To satisfy the required condition, I_{TH}/I_{TH}^{H} should be less than 0.3. Thus, $I_{TH}/I_{TH}^{H} = 0.3$ is the target for low-cost memory chips matching the current production lines.

Table 9.1 Minimum t ensuring the operation window with σ of 10%.

I_{TH}/I_{TH}^{H}	Figure	Minimum t
0.1	Fig. 9.10	0
0.2	Fig. 9.11	1
0.3	Fig. 9.12	3
0.4	Fig. 9.13	7
0.5	Fig. 9.14	larger than 8

Two different MRAM cells have been proposed for decreasing I_{TH}/I_{TH}^{H}. One is the cell that controls the magnetization with the MTJ shape [48][55][56]. This exhibits different magnetization configurations during operation compared with the conventional MRAM cell. As this cell has demonstrated an I_{TH}/I_{TH}^{H} value of 0.29 [48], it is expected to be robust against the half-selected disturbance. The second cell is the toggle cell consisting of a free layer composed of a synthetic antiferromagnet multilayer [57][58][59]. By placing the MTJ with the axis aligned mid-angle between BL and WL, this cell produces a different response to the applied magnetic field than the conventional MRAM, and produces a small I_{TH}/I_{TH}^{H} values that is close to zero [57][58], and then, it does not suffer the half-selected disturbance. Consequently, low-cost memory chips can be realized using these two proposed cells.

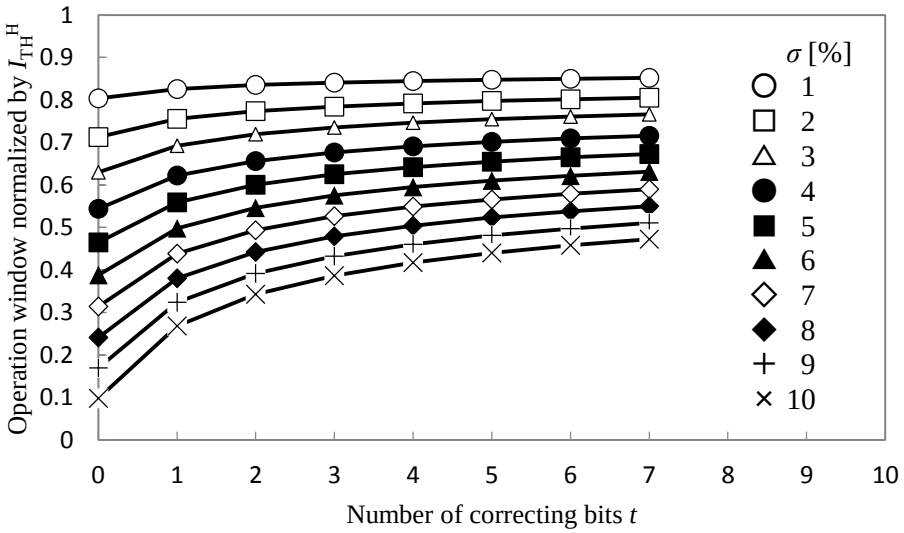


Fig. 9.10 Operation window when $I_{TH}/I_{TH}^{H} = 0.1$.

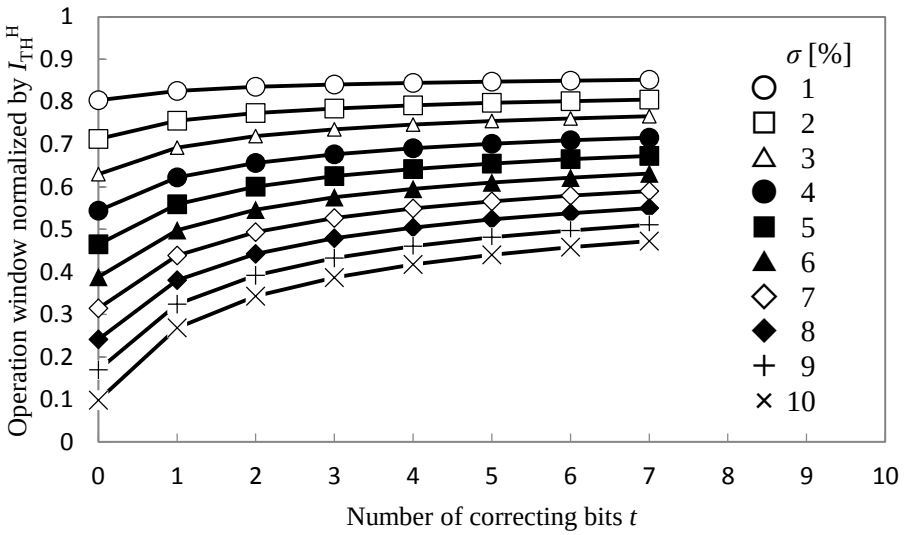


Fig. 9.11 Operation window when $I_{TH}/I_{TH}^{H} = 0.2$.

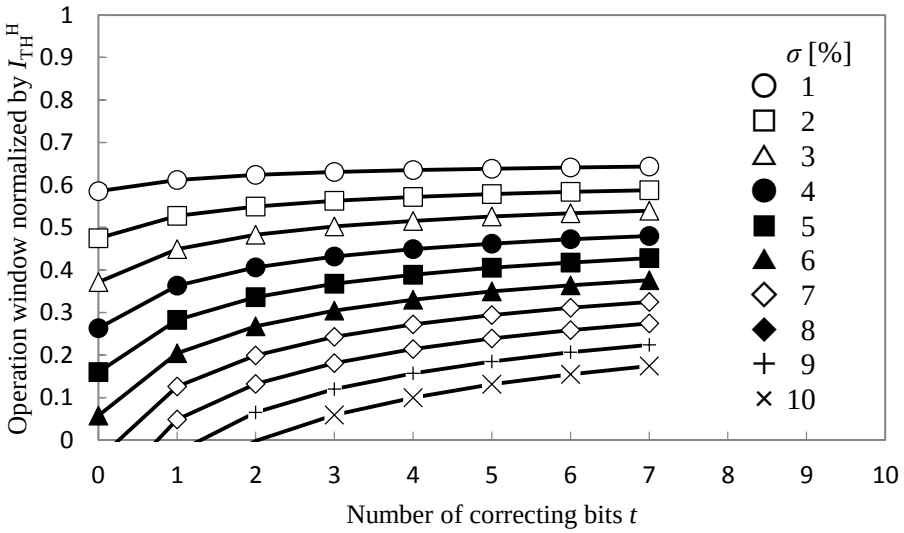


Fig. 9.12 Operation window when $I_{TH}/I_{TH}^{H} = 0.3$.

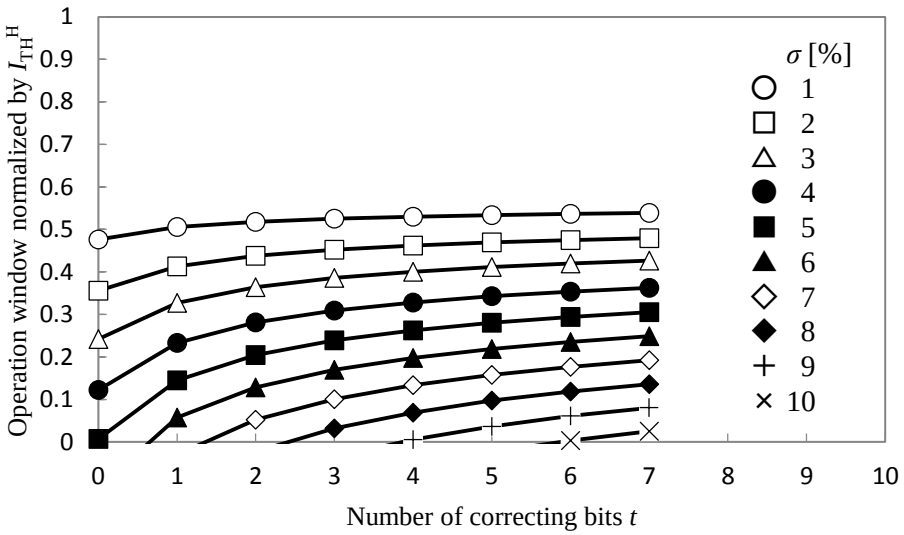


Fig. 9.13 Operation window when $I_{TH}/I_{TH}^{H} = 0.4$.

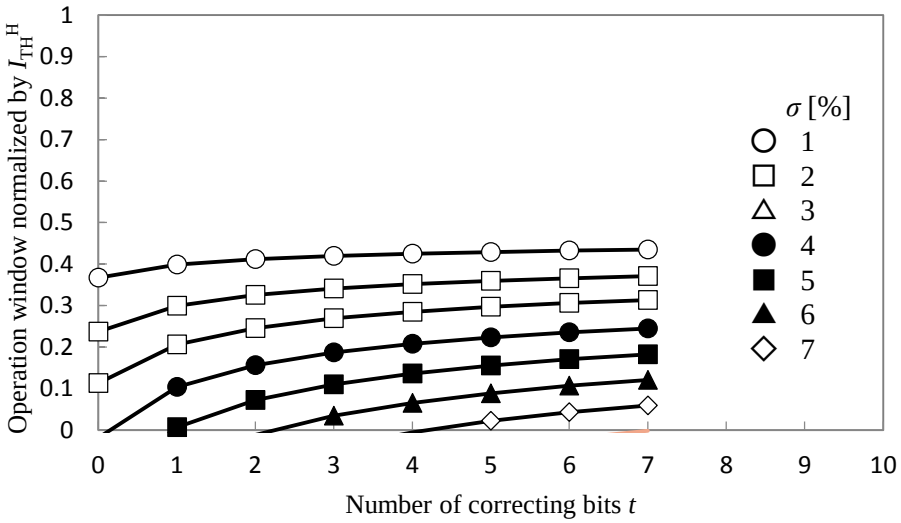


Fig. 9.14 Operation window when $I_{TH}/I_{TH}^{H} = 0.5$.

9.5 Summary

By using the BCH code of length $n = 64$ with $t = 4$, the respective operation windows of the 1 Gb MRAM were calculated as a function of I_{TH}/I_{TH}^{H}. To obtain the operation window with $\sigma = 10\%$, I_{TH}/I_{TH}^{H} should be less than 0.3. This is the target for low-cost memory chips matching the current production lines. Two different MRAM cells have been proposed for decreasing I_{TH}/I_{TH}^{H}. The target I_{TH}/I_{TH}^{H} value can be realized by these two proposed cells.

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C-shape cell with weakly coupled synthetic antiferromagnetic layer," IEEE Transactions on Magnetics, vol. 42, no. 10, pp. 2733−2735, October 2006. doi: 10.1109/TMAG.2006.878854.

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Chapter 10 Conclusions

The facts clarified in the previous chapters are comprehensively discussed to conclude this thesis. The aims of this thesis are to propose BER simulation models for large-scale cross-point memories and to verify their validity for practical purposes. This is because the BER is one of the most important parameters in the design of ECCs for high-density products.

To calculate the BER in cross-point memories, it is necessary to estimate the cell current flowing through the memory array using Kirchhoff's laws. However, it takes a long time to calculate the current when the array size is large. For instance, it takes 33 days to calculate the current in an array with 4096 WLs and 4096 BLs, and then, a simplified circuit has been widely used to speed up the calculation. However, the conventional simplified circuit cannot determine the current at all addresses of the array because it is designed to predict the minimum current due to the wire resistance *IR*-drop.

To overcome this limitation, new simplified circuits are proposed that obtain the current at all addresses of the array. The proposed simplified circuits can calculate the current at the half-selected and non-selected addresses in addition to the selected address. Therefore, the BER due to disturbances can be estimated. These disturbances occur at the half-selected or non-selected addresses while data is being written to the selected address.

The BER models proposed in this thesis use a two-dimensional distribution of two variables: the cell current and the switching threshold current. The probability of the write error is numerically calculated by integrating over the region in which the write current is smaller than the switching threshold current at the selected address. In the same manner, the probability of the disturbance can be obtained by integrating over the region in which the half-selected or the non-selected cell current is larger than the switching threshold current. The proposed simplified circuits constitute effective BER models because they give the current distribution.

By using the proposed BER models, appropriate ECCs were designed for the realization of large-scale cross-point memories.

This thesis now concludes by highlighting the significant results obtained in the previous chapters. As mentioned in Chapter 1, the purpose of this thesis is to present BER simulation models for cross-point memories and to verify their validity for practical purposes. To achieve the purpose, a comprehensive model for estimating the BER caused by disturbances and write errors was proposed in Chapter 3. This is important because the trade-off relationship between the disturbance and the write error is one of the most critical issues in the realization of cross-point memory as a low-cost storage product, as explained in Chapter 7. The model includes the newly proposed simplified circuits for fast calculations of the cell currents as well as a statistical method for estimating the BER of the disturbances and write errors. Using this model, the BER produced by the trade-off relationship between the read disturbances and write errors was precisely predicted for unipolar writing memory. Furthermore, the model was successfully expanded to bipolar writing memory, which suffers from write disturbances in the half-selected and non-selected cells. This is the first attempt to estimate the BER caused by the trade-off relationship between disturbances and write errors in bipolar writing memory as well as in unipolar writing memory. In Chapter 8, the performance of large-scale cross-point memory, in terms of the V_{DD} window, was examined by designing novel circuit parameters. This is a necessary memory design tool for realizing precise memory design and development in a short period. Moreover, the application of the BCH code was shown to reduce the BER to levels that satisfy the production constraints of large-scale memory. In Chapter 9, the device design of MRAM was discussed by estimating the BER that is analogous with the cross-point array. By controlling the threshold curves, large-scale MRAM that satisfies the production constraints can be designed.

The purpose of this thesis is to propose BER simulation models for large-scale cross-point memories and to verify their validity for practical purposes. The conventional method has a limitation: it cannot calculate the BER. The BER models for all types of cross-point memories were established by proposing new simplified circuits. The BER models can calculate the trade-off relationship between the disturbance and the write error, which has not previously been reported. Guides for producing large-scale ReRAM and MRAM were successfully presented by using the BER obtained with the models and the associated ECCs.

The significance of this thesis is that the proposed models are able to estimate the precise BER and design cross-point memory by applying the ECC to give the desired BER. The proposed models can provide BER and ECCs appropriately without manufacturing numerous prototypes, and they can enhance the development of the emerging memories much more effectively.

The originality of this thesis lies in the proposal of new simplified circuits to approximate the current flowing through the non-selected cells. Based on these circuits and statistical methods, BER simulation models were established. The proposed models are comprehensive tools for the design of large-scale cross-point memories.

Because this thesis covers a narrow range of applicable criteria, there is a need for further study in this area. This thesis assumes linear *IV*-curves, steady state, and two-dimensional memories. In the future the proposed models in this thesis will be expanded to non-linear *IV*-curves, transition state, and three-dimensional memories. In an actual device, the non-linear *IV*-curve and the transition phenomenon are often seen. The non-linear *IV*-curve can be applied to Kirchhoff's laws using iterative methods. It is possible to analyze the transition state using capacitance simulation. The three-dimensional memories have already been commercialized in NAND flash memory and PCM, and are becoming the de facto standard. In

the three-dimensional memories, the sneak current increases according to the hierarchy, so it is important to predict the BER caused by disturbance.

By proposing the BER simulation models, this thesis provides the guide to produce the large-scale cross-point memories. This thesis leads to the conclusion that the efficient ECCs are required for the cross-point memories because the trade-off relationship between disturbance and write error is one of the most critical issues to realize the large-scale memories.

Chapter 11 List of research achievements

11.1 Full papers

1. Y. Asao and F. Horiguchi, “A precise model for cross-point memory array,” IEICE Transactions on Electronics, vol. E99−C, no. 1, pp. 119−128, January 2016. doi: 10.1587/transele.E99.C.119.
2. Y. Asao and F. Horiguchi, “A comprehensive model for write disturbance in resistive memory composed of cross-point array,” IEICE Transactions on Electronics, vol. E100−C, no. 3, pp. 329−339, March 2017. doi: 10.1587/transele.E100.C.329.

11.2 International conference papers

1. Y. Asao, S. Hayamizu, Y. Yamada, T. Taguchi, and A. Hiraki, “Effect of strain on bound excitons in high-purity ZnSe bulk and MOCVD homoepitaxially-grown ZnSe Layer,” Materials Research Society Symposium Proceedings, vol. 102, pp. 143−148, December 1987.
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3. Y. Asao, M. Amano, H. Aikawa, T. Ueda, T. Kishi, S. Ikegawa, K. Tsuchida, H. Yoda, T. Kajiyama, Y. Fukuzumi, Y. Iwata, A. Nitayama, K. Shimura, Y. Kato, S. Miura, N. Ishiwata, H. Hada, and S. Tahara, “Design and process integration for high-density, high-speed, and low-power $6F^2$ cross point MRAM cell,” IEEE International Electron Devices Meeting, 2004. Technical Digest, pp. 571–574, December 2004. doi: 10.1109/IEDM.2004.1419224.
4. Y. Asao, M. Iwayama, K. Tsuchida, A. Nitayama, H. Yoda, H. Aikawa, S. Ikegawa, and

T. Kishi, “A statistical model for assessing the fault tolerance of variable switching currents for a 1Gb spin transfer torque magnetoresistive random access memory,” 23th IEEE International Symposium on Defect and Fault Tolerance in VLSI Systems, pp. 507−515, October 2008. doi: 10.1109/DTF.2008.18.

11.3 Co-authored papers

1. T. Nagai, K. Numata, M. Ogihara, M. Shimizu, K. Imai, T. Hara, M. Yoshida, Y. Saito, Y. Asao, S. Sawada, and S. Fujii, “A 17-ns 4-Mb CMOS DRAM,” IEEE Journal of Solid-State Circuits, vol. 26, no. 11, pp. 1538−1543, November 1991. doi: 10.1109/4.98969.
2. T. Kirihata, Y. Watanabe, H. Wong, J. K. DeBrosse, M. Yoshida, D. Kato, S. Fujii, M. R. Wordeman, P. Poechmueller, S. A. Parke, and Y. Asao, “Fault-tolerant designs for 256 Mb DRAM,” IEEE Journal of Solid-State Circuits, vol. 31, no. 4, pp. 558−566, April 1996. doi: 10.1109/4.499733.
3. T. Kirihata, H. Wong, J. K. DeBrosse, Y. Watanabe, T. Hara, M. Yoshida, M. R. Wordeman, S. Fujii, Y. Asao, and B. Krsnik, “Flexible test mode approach for 256-Mb DRAM,” IEEE Journal of Solid-State Circuits, vol. 32, no. 10, pp. 1525−1534, October 1997. doi: 10.1109/4.634660.
4. N. Shimomura, T. Kishi, M. Yoshikawa, E. Kitagawa, Y. Asao, H. Hada, H. Yoda, and S. Tahara, “Edge domain dependent pinning effect by stray field in patterned magnetic tunnel junction,” IEEE Transactions on Magnetics, vol. 41, no. 10, pp. 2652−2654, October 2005. doi: 10.1109/TMAG.2005.854938.
5. N. Shimomura, H. Yoda, S. Ikegawa, T. Kai, M. Amano, H. Aikawa, T. Ueda, M. Nakayama, Y. Asao, K. Hosotani, Y. Shimizu, and K. Tsuchida, “Switching current fluctuation and repeatability for MRAM with propeller-shape MTJ,” IEEE Transactions

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7. H. Yoda, T. Kai, T. Inaba, Y. Iwata, N. Shimomura, S. Ikegawa, K. Tsuchida, Y. Asao, T. Kishi, T. Ueda, S. Takahashi, M. Nagamine, T. Kajiyama, M. Yoshikawa, M. Amano, T. Nagase, K. Hosotani, M. Nakayama, Y. Shimizu, H. Aikawa, K. Nishiyama, E. Kitagawa, R. Takizawa, Y. Ueda, M. Iwayama, and K. Itagaki, "1.8 V power supply 16 Mb-MRAMs with 42.3% array efficiency," IEEE Transactions on Magnetics, vol. 42, no. 10, pp. 2724−2726, October 2006. doi: 10.1109/TMAG.2006.880081.
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10. K. Hosotani, M. Nagamine, T Ueda, H. Aikawa, S. Ikegawa, Y. Asao, H. Yoda and A. Nitayama, "Effect of self-heating on time-dependent dielectric breakdown in ultrathin

MgO magnetic tunnel junctions for spin torque transfer switching magnetic random access memory," Japanese Journal of Applied Physics, vol. 49, no. 4S, pp. 04DD15, April 2010.

11.4 Co-authored international conference presentations

1. S. Hayamizu, Y. Asao, T. Taguchi, and A. Hiraki, "Growth of high-purity ZnSe sigle crystals and characteristics of MOCVD homo-epitaxially grown ZnSe films," Extended Abstracts of the 19th Conference on Solid State Devices and Materials, pp. 255−258, August 1987.
2. T. Nagai, K. Numata, M. Ogihara, M. Shimizu, K. Imai, T. Hara, M. Yoshida, Y. Saito, Y. Asao, S. Sawada, and S. Fujii, "A 17ns 4Mb CMOS DRAM using direct bit-line sensing technique," IEEE International Solid-State Circuits Conference, Digest of Technical Papers, pp. 58, 289−290, February 1991. doi: 10.1109/ISSCC.1991.689063.
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11.5 Presentations in Japanese

1. 浅尾吉昭, 田口常正, 平木昭夫, 新しい THM による ZnSe 単結晶育成およびアクセプター―添加効果, 第 18 回結晶成長国内会議, 富山, 1986 年 8 月.
2. 浅尾吉昭, 木戸口勲, 田口常正, 平木昭夫, THM による大型高純度 ZnSe 単結晶の育成と PL, 第 34 回応用物理学会菅家連合講演会, 早稲田大学, 1987 年 3 月.
3. 浅尾吉昭, 田口常正, 平木昭夫, 再結晶化 THM 法による高純度 ZnSe の育成と浅いアクセプターの応力効果, 電気学会　電子材料研究会, 東京大学, 1987 年 8

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4. 浅尾吉昭, 田口常正, 平木昭夫, ZnSe における束縛励起子の一軸性応力効果, 第 48 回応用物理学会学術講演会, 名古屋大学, 1987 年 10 月.

11.6 United States Patents

No	Patent #	Patent date	Invention
1	5,032,528	1991/7/16	Method of forming a contact hole in semiconductor integrated circuit
2	5,696,401	1997/12/9	Semiconductor device and method of fabricating the same
3	6,278,149	2001/8/21	Plurality of trench capacitors used for the peripheral circuit
4	6,590,244	2003/7/8	Semiconductor memory device using magnetoresistive effect element
5	6,661,689	2003/12/9	Semiconductor memory device
6	6,717,845	2004/4/6	Magnetic memory
7	6,737,691	2004/5/18	Magnetic random access memory
8	6,781,872	2004/8/24	Magnetic memory
9	6,795,334	2004/9/21	Magnetic random access memory
10	6,797,536	2004/9/28	Magnetic memory device having yoke layer, and manufacturing method
11	6,807,094	2004/10/19	Magnetic memory
12	6,831,855	2004/12/14	Magnetic memory
13	6,831,857	2004/12/14	Magnetic memory
14	6,844,204	2005/1/18	Magnetic random access memory
15	6,873,023	2005/3/29	Magnetic random access memory
16	6,879,515	2005/4/12	Magnetic memory device having yoke layer
17	6,882,563	2005/4/19	Magnetic memory device and method for manufacturing the same
18	6,900,490	2005/5/31	Magnetic random access memory
19	6,909,130	2005/6/21	Magnetic random access memory device having high-heat disturbance resistance and high write efficiency
20	6,927,468	2005/8/9	Magnetic random access memory
21	6,934,184	2005/8/23	Magnetic memory
22	6,946,712	2005/9/20	Magnetic memory device using SOI substrate
23	6,947,314	2005/9/20	Magnetic random access memory and method of manufacturing the same
24	6,958,932	2005/10/25	Semiconductor integrated circuit device and method of manufacturing the same
25	6,960,815	2005/11/1	Magnetic memory device having yoke layer, and manufacturing method thereof
26	6,984,865	2006/1/10	Magnetic random access memory
27	7,054,187	2006/5/30	Magnetic memory
28	7,064,402	2006/6/20	Magnetic random access memory
29	7,075,820	2006/7/11	Semiconductor memory device for dynamically storing data with channel body of transistor used as storage node

No	Patent #	Patent date	Invention
30	7,091,539	2006/8/15	Magnetic random access memory
31	7,092,282	2006/8/15	Semiconductor integrated circuit device
32	7,277,318	2007/10/2	Magnetic random access memory and method of manufacturing the same
33	7,333,359	2008/2/19	Magnetic random access memory
34	7,372,118	2008/5/13	Magnetic random access memory and method of manufacturing the same
35	7,376,003	2008/5/20	Magnetic random access memory
36	7,414,879	2008/8/19	Semiconductor memory device
37	7,505,306	2009/3/17	Magnetic memory device
38	7,529,114	2009/5/5	Semiconductor memory device
39	7,579,614	2009/8/25	Magnetic random access memory
40	7,706,175	2010/4/27	Magnetic random access memory and method of manufacturing the same
41	7,727,778	2010/6/1	Magnetoresistive element and method of manufacturing the same
42	7,745,894	2010/6/29	Semiconductor memory device
43	7,751,235	2010/7/6	Semiconductor memory device and write and read methods of the same
44	7,767,469	2010/8/3	Magnetic random access memory and method of manufacturing the same
45	7,781,803	2010/8/24	Semiconductor memory device
46	7,848,136	2010/12/7	Magnetic memory
47	7,869,259	2011/1/11	Resistance change memory, and data write and erase methods thereof
48	7,916,522	2011/3/29	Semiconductor memory device
49	7,919,826	2011/4/5	Magnetoresistive element and manufacturing method thereof
50	7,920,412	2011/4/5	Magnetic random access memory and method of manufacturing the same
51	7,932,513	2011/4/26	Magnetic random access memory, and write method and manufacturing method of the same
52	7,965,542	2011/6/21	Magnetic random access memory and write method of the same
53	7,990,752	2011/8/2	Semiconductor memory
54	8,009,456	2011/8/30	Resistance change type memory
55	8,058,080	2011/11/15	Method of manufacturing a magnetic random access memory, method of manufacturing an embedded memory, and template
56	8,081,505	2011/12/20	Magnetoresistive element and method of manufacturing the same
57	8,111,538	2012/2/7	Semiconductor memory device
58	8,111,540	2012/2/7	Semiconductor memory device
59	8,164,147	2012/4/24	Magnetic random access memory

No	Patent #	Patent date	Invention
60	8,203,193	2012/6/19	Magnetic random access memory and manufacturing method of the same
61	8,309,950	2012/11/13	Semiconductor device and manufacturing method thereof
62	8,314,464	2012/11/20	Semiconductor device and manufacturing method thereof
63	8,513,751	2013/8/20	Semiconductor storage device
64	8,542,519	2013/9/24	Semiconductor memory device
65	8,604,569	2013/12/10	Magnetoresistive element
66	8,644,059	2014/2/4	Semiconductor storage device
67	8,711,602	2014/4/29	Semiconductor memory device
68	8,724,377	2014/5/13	Memory device and method for manufacturing the same
69	8,779,410	2014/7/15	Resistance change memory and method of manufacturing the same
70	8,791,535	2014/7/29	Semiconductor storage device
71	8,829,580	2014/9/9	Magnetoresistive memory and manufacturing method
72	8,941,197	2015/1/27	Magnetic random access memory
73	9,064,792	2015/6/23	Semiconductor storage device
74	9,093,140	2015/7/28	Semiconductor memory device
75	9,165,628	2015/10/20	Semiconductor memory device
76	9,224,786	2015/12/29	Semiconductor storage device
77	9,263,501	2016/2/16	Memory device and method of manufacturing the same
78	9,263,666	2016/2/16	Magnetic random access memory
79	9,368,553	2016/6/14	Memory device
80	9,384,829	2016/7/5	Memory device
81	9,385,160	2016/7/5	Semiconductor storage device

11.7 Japan Patents

No	登録番号	登録日	発明の名称
1	特許第 2726502 号	1997/12/5	半導体装置の製造方法
2	特許第 3100663 号	2000/8/18	半導体装置及びその製造方法
3	特許第 3808802 号	2006/5/26	磁気ランダムアクセスメモリ
4	特許第 3831353 号	2006/7/21	磁気ランダムアクセスメモリ
5	特許第 3866110 号	2006/10/13	磁気メモリ
6	特許第 3871572 号	2006/10/27	磁気記憶装置
7	特許第 3892736 号	2006/12/15	半導体記憶装置
8	特許第 3896072 号	2006/12/22	磁気記憶装置及びその製造方法
9	特許第 3898556 号	2007/1/5	磁気ランダムアクセスメモリ
10	特許第 3906139 号	2007/1/19	磁気ランダムアクセスメモリ
11	特許第 3906145 号	2007/1/19	磁気ランダムアクセスメモリ
12	特許第 3906172 号	2007/1/19	磁気ランダムアクセスメモリおよびその製造方法
13	特許第 3959335 号	2007/5/18	磁気記憶装置及びその製造方法
14	特許第 3964818 号	2007/6/1	磁気ランダムアクセスメモリ
15	特許第 4000000 号	2007/8/17	磁気ランダムアクセスメモリ及びその製造方法
16	特許第 4040414 号	2007/11/16	磁気メモリ
17	特許第 4053825 号	2007/12/14	半導体集積回路装置
18	特許第 4074281 号	2008/2/1	磁気ランダムアクセスメモリ
19	特許第 4080795 号	2008/2/15	磁気メモリ装置
20	特許第 4091328 号	2008/3/7	磁気記憶装置
21	特許第 4146170 号	2008/6/27	磁気ランダムアクセスメモリ
22	特許第 4150047 号	2008/7/4	磁気記憶装置
23	特許第 4157707 号	2008/7/18	磁気メモリ
24	特許第 4322481 号	2009/6/12	半導体集積回路装置
25	特許第 4482039 号	2010/3/26	抵抗変化型メモリ
26	特許第 4516004 号	2010/5/21	磁気記憶装置の製造方法
27	特許第 4533701 号	2010/6/18	磁気メモリ
28	特許第 4538067 号	2010/6/25	半導体記憶装置
29	特許第 4559728 号	2010/7/30	半導体記憶装置
30	特許第 4560025 号	2010/7/30	磁気ランダムアクセスメモリ及びその製造方法
31	特許第 4719208 号	2011/4/8	磁気ランダムアクセスメモリの製造方法
32	特許第 4772845 号	2011/7/1	磁気ランダムアクセスメモリ及びその製造方法
33	特許第 4846817 号	2011/10/21	抵抗変化型メモリ
34	特許第 4922373 号	2012/2/10	半導体装置およびその製造方法
35	特許第 4945592 号	2012/3/9	半導体記憶装置
36	特許第 4991814 号	2012/5/11	半導体装置およびその製造方法
37	特許第 5010650 号	2012/6/8	磁気抵抗メモリ
38	特許第 5019223 号	2012/6/22	半導体記憶装置
39	特許第 5091495 号	2012/9/21	磁気ランダムアクセスメモリ
40	特許第 5100514 号	2012/10/5	半導体メモリ
41	特許第 5165898 号	2012/12/28	磁気ランダムアクセスメモリ及びその書き込み方法
42	特許第 5502635 号	2014/3/20	半導体記憶装置

No	登録番号	登録日	発明の名称
43	特許第 5551129 号	2014/5/30	記憶装置
44	特許第 5677186 号	2015/1/9	半導体記憶装置
45	特許第 5677187 号	2015/1/9	半導体記憶装置
46	特許第 5740225 号	2015/5/1	抵抗変化メモリの製造方法
47	特許第 5934086 号	2016/5/13	記憶装置

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Glossary

[1] **Semiconductor memory** is an electronic data storage device implemented on semiconductor circuits.

[2] **Integrated circuit (IC)** is a set of electronic circuits on a silicon substrate having transistors and other electronic components in a certain area.

[3] **Dynamic random access memory (DRAM)** is a type of random access memory that stores data in a capacitor and periodically requires a refresh cycle to retain the stored data. Random access memory is a form of computer data storage allowing data to be read or written at the same time irrespective of the memory address. DRAM is a volatile memory because the stored data in the capacitor disappear after the power supply is switched off.

[4] **NAND Flash memory** is a solid state non-volatile computer storage medium that is electrically programmed.

[5] **Central processing unit (CPU)** is an electronic circuit in a computer that processes the order of a computer program.

[6] **Hard disc drive (HDD)** is a type of data storage device that reads and writes data by rotating disks coated with magnetic films and moving magnetic heads.

[7] **Static random access memory (SRAM)** is a type of random access memory that stores data in a flip-flop and does not require a refresh cycle. SRAM is a volatile memory because the stored data in the flip-flop disappear after the power supply is switched off.

[8] **Cache memory** is a memory that is implemented in CPU and stores frequently used data to reduce access to the main memory and realize high-speed computation.

[9] **Wafer** is a thin substrate that is used for manufacturing integrated circuits. It is often made of silicon, which is called silicon wafer.

[10] **Compact disc (CD)** is a type of media that records digital information.

[11] **Digital versatile disc (DVD)** is a type of media that records digital information.

[12] **Blue-ray disc (BD)** is a type of media that records digital information.

[13] **Volatile memory** is a type of semiconductor memory that cannot retain stored information after the power is switched off.

[14] **Non-volatile memory** is a type of semiconductor memory that can retain stored information after the power is switched off.

[15] **Block** is a unit of Flash memory data consisting of several pages, e.g., 64 pages. The page is a unit of data that consists of several bytes, e.g., 2048 bytes + 64 bytes.

[16] **NOR Flash memory** is a solid state non-volatile computer storage medium that is electrically programmed.

[17] **Solid state drive (SSD)** is a data storage device used in a computer that is designed to access data in the same way as hard disk drives.

[18] **Phase-change memory (PCM)** is a type of resistance-change memory that works as a random access memory. The memory element usually consists of $Ge_2Sb_2Te_5$. It can be transformed between crystal and amorphous phases by applying an electric current. Crystal and amorphous phases show low and high resistance values, respectively.

[19] **Resistive random access memory (ReRAM)** is a type of resistance-change memory that works as a random access memory. A variety of phenomena have been observed in this type, such as the electrochemical effect, redox effect, and thermo-chemical effect.

[20] **Magnetic random access memory (MRAM)** is a type of resistance-change memory that works as a random access memory. This memory uses the magnetoresistance effect in a magnetic tunnel junction (MTJ).

[21] **SET** is a write operation that makes the resistance of a memory element low.

[22] **RESET** is a write operation that makes the resistance of a memory element high.

[23] **Bit error rate (BER)** is the probability that a failing bit occurs inside a semiconductor memory chip.

[24] **Error correcting code (ECC)** is an algorithm that detects and corrects errors.

[25] **MPU (Micro Processing Unit)** is a semiconductor chip that operates a computer.

[26] **High-resistance state (HRS)** is a state whereby a memory element of resistance-change memories, such as ReRAM and PcRAM, shows higher resistance when the memory element has two resistance states. The other state is the low-resistance state (LRS).

[27] **Low-resistance state (LRS)** is a state whereby a memory element of resistance-change memories, such as ReRAM and PcRAM, shows lower resistance when the memory element has two resistance states. The other state is the high-resistance state (HRS).

[28] **Monte Carlo method** is a technique in which numerical calculations are carried out using random numbers.

[29] **Chi-square test** is a statistical test that checks the fit of data to a theoretical distribution.

[30] **Degrees of freedom** are values in a statistical calculation that are free to vary.

[31] **Significance level** is a statistical criterion that rejects the null hypothesis. Generally, 5% and 1% significance levels are used. If the significance level of 5% is used for the null hypothesis, there is a 5% possibility that the hypothesis will be rejected although it is correct.

[32] **Tunnel magnetoresistance (TMR) effect** is a magnetoresistive effect that occurs in a magnetic tunnel junction, where an insulator is sandwiched by two ferromagnets. The electrical resistance of the MTJ varies with the applied magnetic field.

[33] **Metal–oxide–semiconductor field-effect transistor (MOSFET)** is a type of field-effect transistor (FET) consisting of an insulated gate and substrate. The applied voltage on the gate determines the conductivity of the transistor.